DFI

SH960MD-CM236/QM170/HM170

COM Express Basic Module
User's Manual

Preliminary Version

Copyright

Trademarks

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

1. The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
2. Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website, or acquired as an electronic file included in the optional CD/DVD. The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

1. Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.

2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.

3. Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.

4. We will not be liable for any indirect, special, incidental or consequencial damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

1. To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.

2. Wear an antistatic wrist strap.

3. Do all preparation work on a static-free surface.

4. Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.

5. Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.

- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One SH960MD-CM236/QM170/HM170 board
- CPU Cooler

Optional Items

- COM332-B carrier board kit
- Heat spreader

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.
If you are installing the system board in a new system, you will need at least the following internal components.

- Monitor
- USB keyboard
- Storage device such as hard disk drive, CD-ROM, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

▶ Specifications

SYSTEM	Processor	6th Generation Intel® Core™ Processors, BGA 1440 - Xeon® E3-1515M v5 Processor, Quad Core, 8M Cache, 2.8GHz (3.7GHz), 45W (Support ECC) - Core™ i7-6820EQ Processor, Quad Core, 8M Cache, 2.8GHz (3.5GHz), 45W - Core™ i5-6442EQ Processor, Quad Core, 6M Cache, 1.9GHz (2.7GHz), 25W - Core™ i3-6100E Processor, Dual Core, 3M Cache, 2.7GHz, 35W (Support ECC) - Celeron® Processor G3900E, Dual Core, 2M Cache, 2.4GHz, 35W (Support ECC)
	Chipset	Intel® CM236/QM170/HM170
	Memory	- 8GB/16GB DDR4 Memory Down - Dual Channel DDR4 2133MHz - ECC (CPU dependent)
	BIOS	Insyde SPI 128Mbit
GRAPHICS	Controller	Intel® HD Graphics
	Feature	OpenGL up to 4.4, DirectX 12, OpenCL 2.1 HW Decode: AVC/H.264, MPEG2, VC1/WMV9, JPEG/MJPEG, HEVC/H265, VP8, VP9 HW Encode: AVC/H.264, MPEG2, JPEG, HEVC/H265, VP8, VP9
	Display	1 x VGA/DDI (DDI available upon request) 1 x LVDS/eDP (eDP available upon request) 2 x DDI (HDMI/DVI/DP++)
	Resolution	VGA: resolution up to 1920x1200 @ 60Hz LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz HDMI: resolution up to 4096x2160 @ 24Hz or 2560x1600 @ 60Hz DVI: resolution up to 1920x1200 @ 60Hz DP++/eDP: resolution up to 4096x2304 @ 60Hz
	Triple Displays	VGA + LVDS + DDI, VGA + DDI1 + DDI2 eDP + 2 DDI (available upon request)
EXPANSION	Interface	1 x PCIe x16 or 2 x PCIe x8 (Gen 3) 8 x PCIe x1 or 2 x PCIe x4 or 4 x PCIe x2 (Gen 3) 1 x LPC 1 x I^2C 1 x SMBus 2 x UART (TX/RX)
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x Intel® I210IT (10/100/1000Mbps)

I/O	USB	4 x USB 3.0 8 x USB 2.0
	SATA	4 x SATA 3.0 (up to 6Gb/s) RAID 0/1/5/10
	DIO	1 x 8-bit DIO
WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
SECURITY	TPM	Available Upon Request
POWER	Type	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)
OS SUPPORT		Windows 8.1 64-bit Windows 7 (/WES7) 32/64-bit Windows 10 IoT Enterprise 64-bit Debian 8 (with VESA graphic driver) CentOS 7 (with VESA graphic driver) Linux
ENVIRONMENT	Temperature	Operating: 0 to 60°C; Storage: -40 to 85°C
	Humidity	Operating: 5 to 90% RH; Storage: 5 to 90% RH
MECHANICAL	Dimensions	COM Express® Basic: 95mm (3.74") x 125mm (4.9")
	Compliance	PICMG COM Express® R2.1, Type 6

▶ Features

Watchdog Timer

The Watchdog Timer function allows your application to regularly “clear” the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

DDR4

DDR4 delivers increased system bandwidth and improves performance. The advantages of DDR4 provide an extended battery life and improve the performance at a lower power than DDR3/DDR2. Instead of using memory connectors, the system features memory down with the support of ECC memory.

Graphics

The integrated Intel® HD graphics engine delivers an excellent blend of graphics performance and features to meet business needs. It provides excellent video and 3D graphics with outstanding graphics responsiveness. These enhancements deliver the performance and compatibility needed for today’s and tomorrow’s business applications. Supports VGA, LVDS, eDP and DDI display outputs.

Serial ATA

The system supports multiple SATA 3.0 (up to 6Gb/s) ports and allows for different configurations of RAID levels to meet various requirements for data redundancy and performance.

Gigabit LAN

The Intel® I210IT Gigabit LAN controller features up to 1Gbps data transmission with support for Intel® Active Management Technology. It provides remote maintenance and manageability for networked computing assets in an enterprise environment.

Wake-On-LAN

This feature allows the network to remotely wake up a Soft Power Down (Soft-Off) PC. It is supported via the onboard LAN port or via a PCI LAN card that uses the PCI PME (Power Management Event) signal. However, if your system is in the Suspend mode, you can power-on the system only through an IRQ or DMA interrupt.

USB

The system board supports the new USB 3.0. It is capable of running at a maximum transmission speed of up to 5 Gbit/s (625 MB/s) and is faster than USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12Mb/s). USB 3.0 reduces the time required for data transmission, reduces power consumption, and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

ACPI STR

The system board is designed to meet the ACPI (Advanced Configuration and Power Interface) specification. ACPI has energy saving features that enables PCs to implement Power Management and Plug-and-Play with operating systems that support OS Direct Power Management. ACPI when enabled in the Power Management Setup will allow you to use the Suspend to RAM function.
With the Suspend to RAM function enabled, you can power-off the system at once by pressing the power button or selecting “Standby” when you shut down Windows® without having to go through the sometimes tiresome process of closing files, applications and operating system. This is because the system is capable of storing all programs and data files during the entire operating session into RAM (Random Access Memory) when it powers-off. The operating session will resume exactly where you left off the next time you power-on the system.

Power Failure Recovery

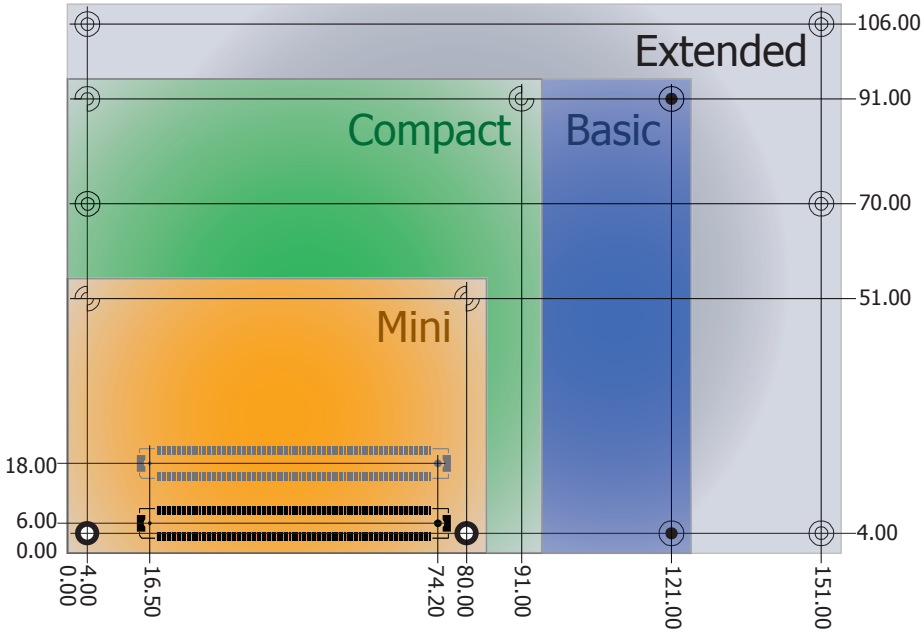
When power returns after an AC power failure, you may choose to either power-on the system manually or let the system power-on automatically.

▶ Concept

COM Express

Computer-on-module (COM) Express is a PC form factor designed with the core computing integrated on a fairly compact module. All the I/O signals and power supply are concentrated and mapped to the board-to-board connectors on the bottom side to interface with a carrier board that is typically customized to fit the application. When an upgrade or change of application is needed, the physical separation of the core computing and the I/O of COM Express cuts back the cost greatly, whereas canonical IPC designs would typically require an entire makeover. The COM Express module can be replaced when there is only need to upgrade for higher computing performance, while the carrier board can be redesigned when there is solely change in application. COM Express also comes in different form factors and signal Types cut out for different scales and aspects of the system's application. Detailed specifications of COM Express are available on the website of PCI Industrial Computer Manufacturers Group (PICMG).

- Common for all Form Factors
- Extended only
- Basic only
- Compact only
- Compact and Basic only
- Mini only



Carrier Board

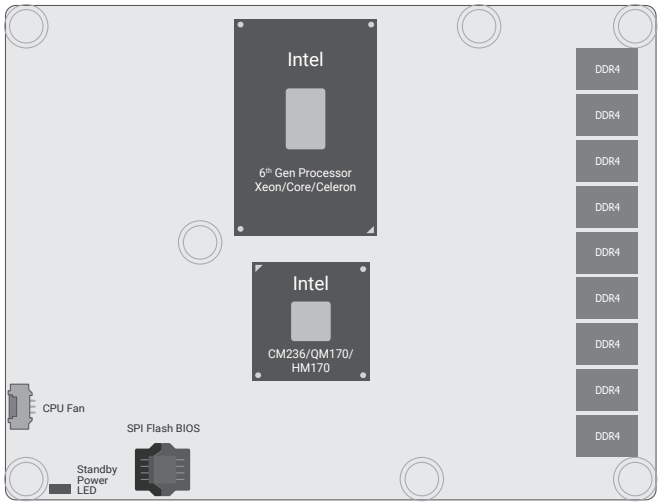
The design of a carrier board for COM Express greatly depends on the form factor and signal Type of the COM Express module. The carrier board typically handles — but not limited to — one COM Express module, and is populated with stand-offs that conform to the form factor of the module's mounting holes.

SH960MD is a Type 6 COM Express (R2.1) module compatible with DFI's proprietary carrier board — COM332-B — as an optional item. If the carrier board is to be customized, the design guide for the carrier board can be attained via the Partner Zone page on our website.

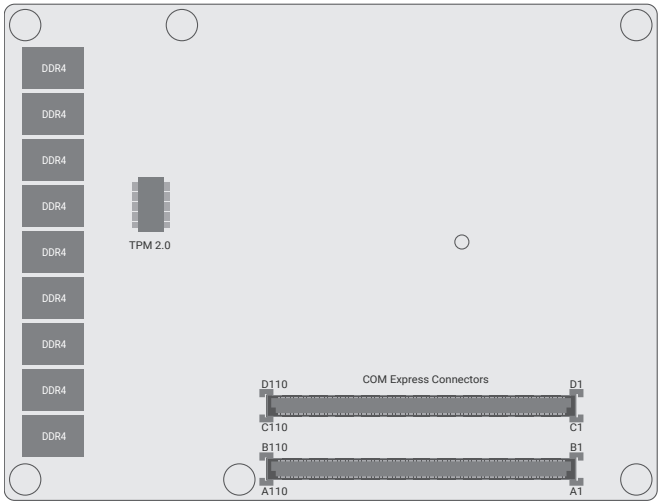
Chapter 2 - Hardware Installation

▶ Board Layout

Top View

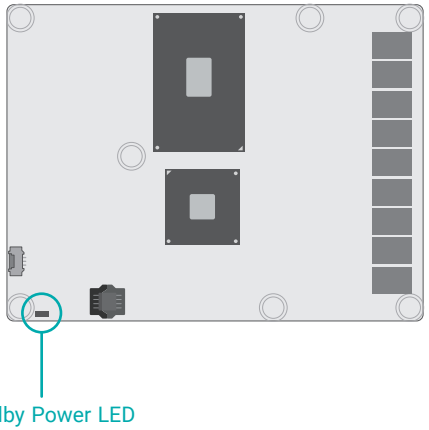


Bottom View



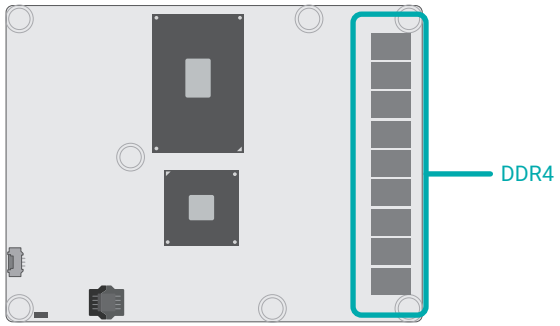
Important:
Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

▶ Standby Power LED



Important:
When the Standby Power LED lights red, it indicates that there is power on the system board. Power-off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the motherboard and components.

▶ System Memory



The system board supports the following memory interface.

Single Channel (SC)
Data will be accessed in chunks of 64 bits from the memory channels.

Dual Channel (DC)
Data will be accessed in chunks of 128 bits from the memory channels. Dual channel provides better system performance because it doubles the data transfer rate.

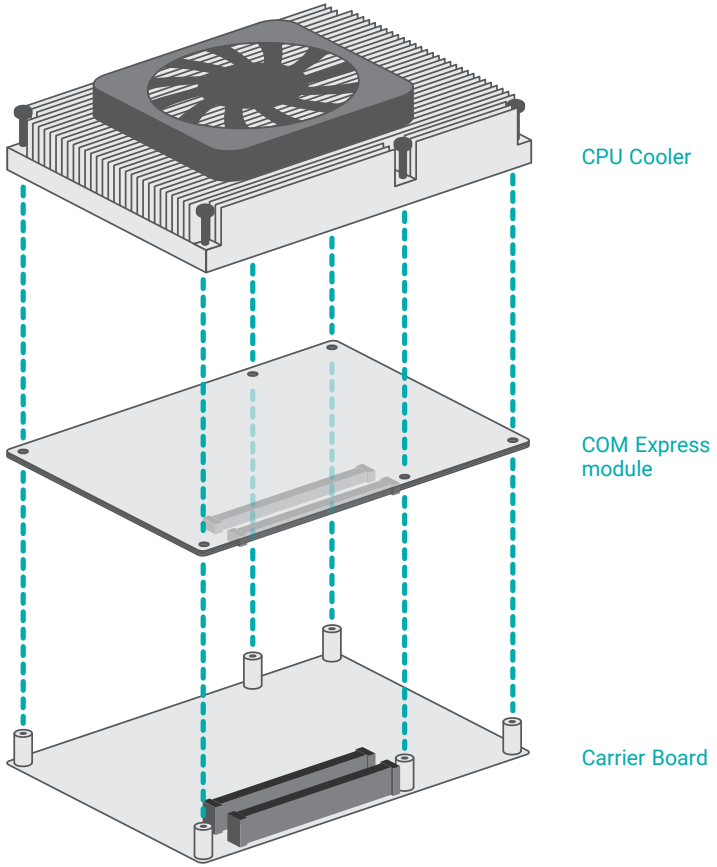
Single Channel	DIMMs are on the same channel. DIMMs in a channel can be identical or completely different. However, we highly recommend using identical DIMMs. Not all slots need to be populated.
Dual Channel	DIMMs of the same memory configuration are on different channels.

Features

- DDR4 2133MHz memory
- ECC (only available with certain options, see Specifications)
- Dual channel memory interface

▶ Assembly

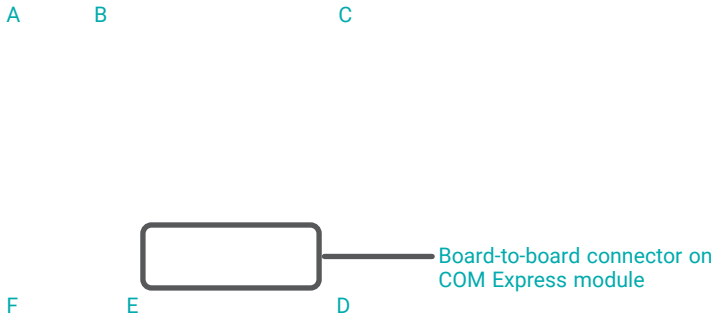
A CPU cooler is included in the standard package. The CPU cooler contains six spring screws and shall be installed after the COM Express module is securely mounted onto the carrier board. Please make sure the cooler, the module, and the carrier board are oriented correctly by inspecting whether the screws, screw holes, and stand-offs all align.

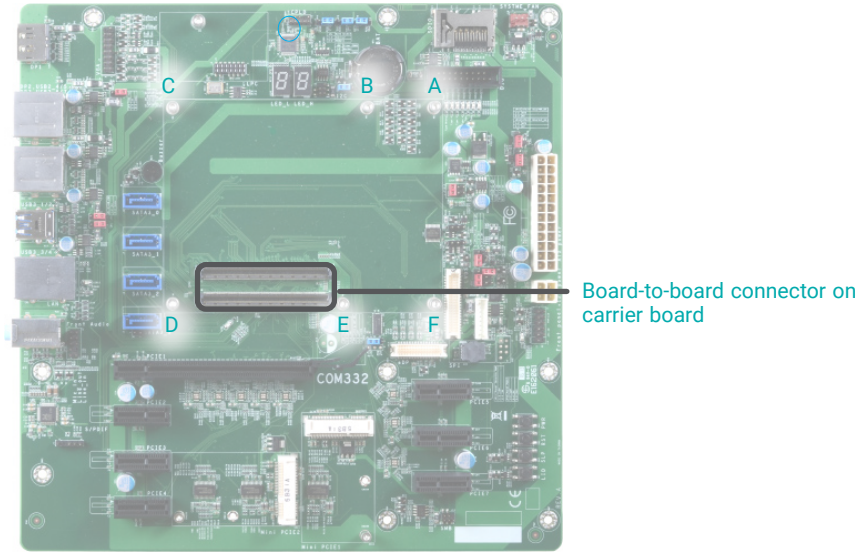


Note:
The carrier board is not included in the standard package and is typically customized.

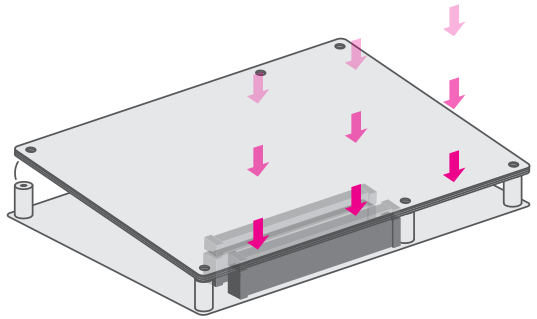
Assembly

1. Locate the COM Express board-to-board connectors on the bottom side of the module and the carrier board. Locate the mounting holes on the module and the corresponding stand-offs on the carrier board.

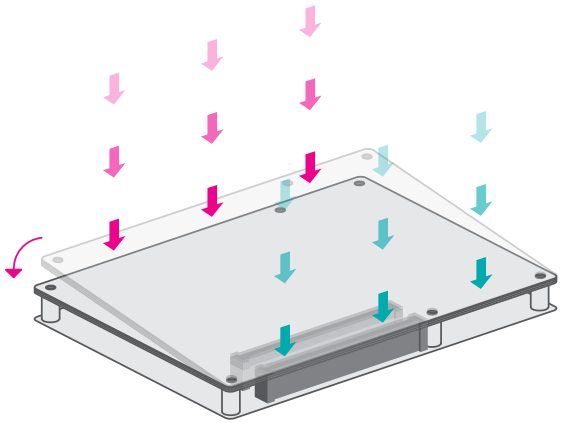




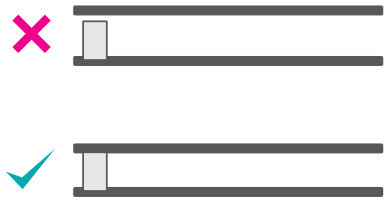
2. Place the module on the carrier board while making sure the mounting holes and connectors all align. At the long edge of the module closer to the connector, apply firm pressure onto the module and press it onto the the carrier board until the three stand-offs and the edge of the module close up. The other edge of the module away from the connector may still remain slightly aloft from the stand-offs at this moment.



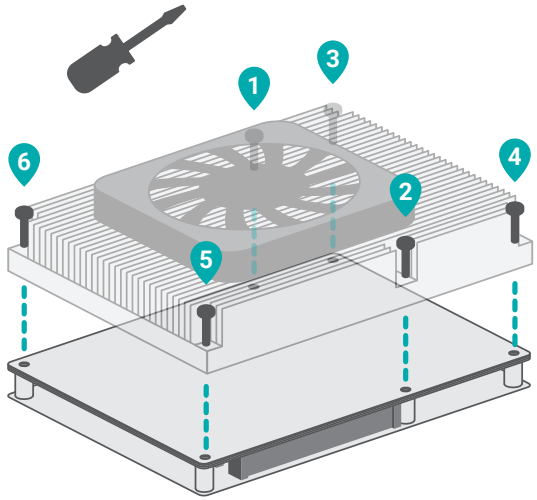
3. At the long edge away from the connector, apply firm pressure with another hand onto the module and press it onto the carrier board until the module is against the remaining three stand-offs. Please also maintain the pressure described in the previous step the whole time.



4. Inspect whether the gaps between the module and the stand-offs all close up. It is highly recommended that the module be removed and installed again following the previous steps when there is discernable gap.



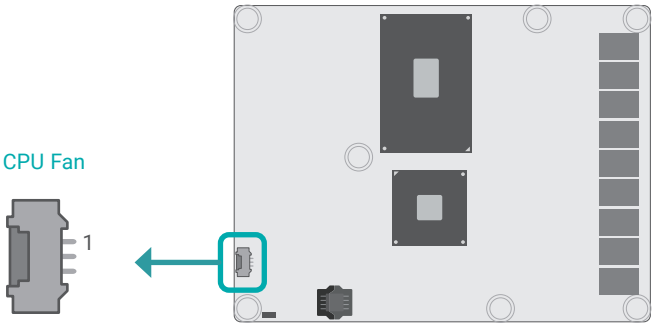
5. Place the CPU cooler, i.e. heatsink and fan, onto the module while making sure the screws on the cooler align with the screw holes on the module. The thermal interface metals underneath the cooler should also sit directly on top of the CPU and PCH chipsets on the module. Use a screw driver to fasten the screws in the order as numbered below. By following the order, the risk of damaging the component is significantly reduced.



▶ I/O Connectors

CPU Fan

■ CPU Fan



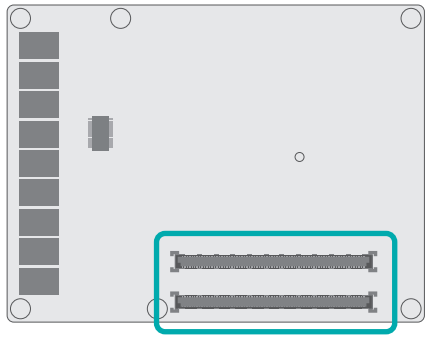
The fan connector is used to connect to cooling fans. Cooling fans provide adequate air circulation throughout the chassis and dissipate heat to prevent overheating of the system board and components.

BIOS Setting
Fan speed can be read in the Advanced menu (“SIO ITE8528E” submenu) of the BIOS. Refer to chapter 3 for more information.

■ 3-pin Fan Pin Assignment

Pin	Assignment
1	Ground
2	Power
3	Sense

Board-to-board Connector



The two board-to-board connectors are located at the bottom side of the COM Express module. Four rows (row A to row D) of pins and their signal are specified as listed below.

Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#
A4	GBE0_LINK100#	B4	LPC_AD0
A5	GBE0_LINK1000#	B5	LPC_AD1
A6	GBE0_MDI2-	B6	LPC_AD2
A7	GBE0_MDI2+	B7	LPC_AD3
A8	GBE0_LINK#	B8	LPC_DRQ0#
A9	GBE0_MDI1-	B9	LPC_DRQ1#
A10	GBE0_MDI1+	B10	LPC_CLK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	NC	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	SATA2_TX+	B22	SATA3_TX+
A23	SATA2_TX-	B23	SATA3_TX-
A24	SUS_S5#	B24	PWR_OK
A25	SATA2_RX+	B25	SATA3_RX+
A26	SATA2_RX-	B26	SATA3_RX-
A27	BATLOW#	B27	WDT
A28	(S)ATA_ACT#	B28	NC
A29	AC/HDA_SYNC	B29	AC/HDA _SDIN1
A30	AC/HDA _RST#	B30	AC/HDA _SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	AC/HDA _BITCLK	B32	SPKR
A33	AC/HDA _SDOUT	B33	I2C_CK
A34	BIOS_DIS0#	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	EXCD1_PERST#
A48	EXCD0_PERST#	B48	EXCD1_CPPE#
A49	EXCD0_CPPE#	B49	SYS_RESET#
A50	LPC_SERIRQ	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+
A53	PCIE_TX5-	B53	PCIE_RX5-
A54	GPI0	B54	GPO1
A55	PCIE_TX4+	B55	PCIE_RX4+
A56	PCIE_TX4-	B56	PCIE_RX4-
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+/eDP_TX2+ (opt.)	B71	LVDS_B0+
A72	LVDS_A0-/eDP_TX2- (opt.)	B72	LVDS_B0-
A73	LVDS_A1+/eDP_TX1+ (opt.)	B73	LVDS_B1+
A74	LVDS_A1-/eDP_TX1- (opt.)	B74	LVDS_B1-
A75	LVDS_A2+/eDP_TX0+ (opt.)	B75	LVDS_B2+
A76	LVDS_A2-/eDP_TX0- (opt.)	B76	LVDS_B2-

Row A		Row B	
A77	LVDS_VDD_EN/eDP_VDD_EN (opt.)	B77	LVDS_B3+
A78	LVDS_A3+	B78	LVDS_B3-
A79	LVDS_A3-	B79	LVDS_BKLT_EN/eDP_BKLT_EN (opt.)
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+/eDP_TX3+ (opt.)	B81	LVDS_B_CK+
A82	LVDS_A_CK-/eDP_TX3- (opt.)	B82	LVDS_B_CK-
A83	LVDS_I2C_CK/eDP_AUX+ (opt.)	B83	LVDS_BKLT_CTRL/eDP_BKLT_CTRL (opt.)
A84	LVDS_I2C_DAT/eDP_AUX- (opt.)	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	RSVD/eDP_HPD	B87	VCC_5V_SBY
A88	PCIE0_CLK_REF+	B88	BIOS_DIS1#
A89	PCIE0_CLK_REF-	B89	VGA_RED
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	VGA_GRN
A92	SPI_MISO	B92	VGA_BLU
A93	GPO0	B93	VGA_HSYNC
A94	SPI_CLK	B94	VGA_VSYNC
A95	SPI_MOSI	B95	VGA_I2C_CK
A96	TPM_PP	B96	VGA_I2C_DAT
A97	NC	B97	SPI_CS#
A98	SER0_TX	B98	RSVD
A99	SER0_RX	B99	RSVD
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWMOUT
A102	SER1_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)
C2	GND	D2	GND
C3	USB_SSRX0-	D3	USB_SSTX0-
C4	USB_SSRX0+	D4	USB_SSTX0+
C5	GND	D5	GND
C6	USB_SSRX1-	D6	USB_SSTX1-
C7	USB_SSRX1+	D7	USB_SSTX1+
C8	GND	D8	GND
C9	USB_SSRX2-	D9	USB_SSTX2-
C10	USB_SSRX2+	D10	USB_SSTX2+
C11	GND (FIXED)	D11	GND (FIXED)
C12	USB_SSRX3-	D12	USB_SSTX3-
C13	USB_SSRX3+	D13	USB_SSTX3+
C14	GND	D14	GND
C15	NC	D15	DDI1_CTRLCLK_AUX+
C16	NC	D16	DDI1_CTRLDATA_AUX-
C17	RSVD	D17	RSVD

Row C		Row D	
C18	RSVD	D18	RSVD
C19	PCIE_RX6+	D19	PCIE_TX6+
C20	PCIE_RX6-	D20	PCIE_TX6-
C21	GND (FIXED)	D21	GND (FIXED)
C22	PCIE_RX7+	D22	PCIE_TX7+
C23	PCIE_RX7-	D23	PCIE_TX7-
C24	DDI1_HPD	D24	RSVD
C25	NC	D25	RSVD
C26	NC	D26	DDI1_PAIR0+
C27	RSVD	D27	DDI1_PAIR0-
C28	RSVD	D28	RSVD
C29	NC	D29	DDI1_PAIR1+
C30	NC	D30	DDI1_PAIR1-
C31	GND (FIXED)	D31	GND (FIXED)
C32	DDI2_CTRLCLK_AUX+	D32	DDI1_PAIR2+
C33	DDI2_CTRLDATA_AUX-	D33	DDI1_PAIR2-
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL
C35	RSVD	D35	RSVD
C36	DDI3_CTRLCLK_AUX+	D36	DDI1_PAIR3+
C37	DDI3_CTRLDATA_AUX-	D37	DDI1_PAIR3-
C38	DDI3_DDC_AUX_SEL	D38	RSVD
C39	DDI3_PAIR0+	D39	DDI2_PAIR0+
C40	DDI3_PAIR0-	D40	DDI2_PAIR0-
C41	GND (FIXED)	D41	GND (FIXED)
C42	DDI3_PAIR1+	D42	DDI2_PAIR1+
C43	DDI3_PAIR1-	D43	DDI2_PAIR1-
C44	DDI3_HPD	D44	DDI2_HPD
C45	RSVD	D45	RSVD
C46	DDI3_PAIR2+	D46	DDI2_PAIR2+
C47	DDI3_PAIR2-	D47	DDI2_PAIR2-
C48	RSVD	D48	RSVD
C49	DDI3_PAIR3+	D49	DDI2_PAIR3+
C50	DDI3_PAIR3-	D50	DDI2_PAIR3-
C51	GND (FIXED)	D51	GND (FIXED)
C52	PEG_RX0+	D52	PEG_TX0+
C53	PEG_RX0-	D53	PEG_TX0-
C54	NC	D54	PEG_LANE_RV#
C55	PEG_RX1+	D55	PEG_TX1+
C56	PEG_RX1-	D56	PEG_TX1-
C57	NC	D57	GND
C58	PEG_RX2+	D58	PEG_TX2+
C59	PEG_RX2-	D59	PEG_TX2-
C60	GND (FIXED)	D60	GND (FIXED)
C61	PEG_RX3+	D61	PEG_TX3+
C62	PEG_RX3-	D62	PEG_TX3-
C63	RSVD	D63	RSVD
C64	RSVD	D64	RSVD
C65	PEG_RX4+	D65	PEG_TX4+
C66	PEG_RX4-	D66	PEG_TX4-
C67	NC	D67	GND
C68	PEG_RX5+	D68	PEG_TX5+
C69	PEG_RX5-	D69	PEG_TX5-
C70	GND (FIXED)	D70	GND (FIXED)
C71	PEG_RX6+	D71	PEG_TX6+

Row C		Row D	
C72	PEG_RX6-	D72	PEG_TX6-
C73	GND	D73	GND
C74	PEG_RX7+	D74	PEG_TX7+
C75	PEG_RX7-	D75	PEG_TX7-
C76	GND	D76	GND
C77	RSVD	D77	RSVD
C78	PEG_RX8+	D78	PEG_TX8+
C79	PEG_RX8-	D79	PEG_TX8-
C80	GND (FIXED)	D80	GND (FIXED)
C81	PEG_RX9+	D81	PEG_TX9+
C82	PEG_RX9-	D82	PEG_TX9-
C83	RSVD	D83	RSVD
C84	GND	D84	GND
C85	PEG_RX10+	D85	PEG_TX10+
C86	PEG_RX10-	D86	PEG_TX10-
C87	GND	D87	GND
C88	PEG_RX11+	D88	PEG_TX11+
C89	PEG_RX11-	D89	PEG_TX11-
C90	GND (FIXED)	D90	GND (FIXED)
C91	PEG_RX12+	D91	PEG_TX12+
C92	PEG_RX12-	D92	PEG_TX12-
C93	GND	D93	GND
C94	PEG_RX13+	D94	PEG_TX13+
C95	PEG_RX13-	D95	PEG_TX13-
C96	GND	D96	GND
C97	RSVD	D97	RSVD
C98	PEG_RX14+	D98	PEG_TX14+
C99	PEG_RX14-	D99	PEG_TX14-
C100	GND (FIXED)	D100	GND (FIXED)
C101	PEG_RX15+	D101	PEG_TX15+
C102	PEG_RX15-	D102	PEG_TX15-
C103	GND	D103	GND
C104	VCC_12V	D104	VCC_12V
C105	VCC_12V	D105	VCC_12V
C106	VCC_12V	D106	VCC_12V
C107	VCC_12V	D107	VCC_12V
C108	VCC_12V	D108	VCC_12V
C109	VCC_12V	D109	VCC_12V
C110	GND (FIXED)	D110	GND (FIXED)

▶ Signal Descriptions

Pin Types

I Input to the Module
O Output from the Module
I/O Bi-directional input / output signal
OD Open drain output
RSVD pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

HDA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
HDA_RST#	A30	O CMOS	3.3V Suspend/3.3V	series 33Ω resistor	Reset output to CODEC, active low.	CODEC Reset.
HDA_SYNC	A29	O CMOS	3.3V/3.3V	series 33Ω resistor	Sample-synchronization signal to the CODEC(s).	Serial Sample Rate Synchronization.
HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V	series 33Ω resistor	Serial data clock generated by the external CODEC(s).	24 MHz Serial Bit Clock for HDA CODEC.
HDA_SDOUT	A33	O CMOS	3.3V/3.3V	series 33Ω resistor	Serial TDM data output to the CODEC.	Audio Serial Data Output Stream.
HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Serial TDM data inputs from up to 3 CODECs.	Audio Serial Data Input Stream from CODEC[0:2].
HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V			
HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V	NC		

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend		Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-	Media Dependent Interface (MDI) differential pair 0.
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend			
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend			Media Dependent Interface (MDI) differential pair 1.
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend			
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend			Media Dependent Interface (MDI) differential pair 2. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend			
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend			Media Dependent Interface (MDI) differential pair 3. Only used for 1000Mbit/sec Gigabit Ethernet mode.
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 activity indicator, active low.	Ethernet controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 link indicator, active low.	Ethernet controller 0 link indicator, active low.
GBE0_ LINK100#	A4	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.	Ethernet controller 0 100Mbit/sec link indicator, active low.
GBE0_ LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.	Ethernet controller 0 1000Mbit/sec link indicator, active low.
GBE0_CTREF	A14	REF	GND min 3.3V max	NC	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.	Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap.

SATA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 0 transmit differential pair.	Serial ATA channel 0 Transmit output differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 0 receive differential pair.	Serial ATA channel 0 Receive input differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 1 transmit differential pair.	Serial ATA channel 1 Transmit output differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 1 receive differential pair.	Serial ATA channel 1 Receive input differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA2_TX+	A22	O SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 2 transmit differential pair.	Serial ATA channel 2 Transmit output differential pair.
SATA2_TX-	A23	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA2_RX+	A25	I SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 2 receive differential pair.	Serial ATA channel 2 Receive input differential pair.
SATA2_RX-	A26	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA3_TX+	B22	O SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 3 transmit differential pair.	Serial ATA channel 3 Transmit output differential pair.
SATA3_TX-	B23	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA3_RX+	B25	I SATA	AC coupled on Module	AC Coupling capacitor	Serial ATA or SAS Channel 3 receive differential pair.	Serial ATA channel 3 Receive input differential pair.
SATA3_RX-	B26	I SATA	AC coupled on Module	AC Coupling capacitor		
(S)ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 10KW to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.	Serial ATA activity LED. Open collector output pin driven during SATA command activity.

PCI Express Lanes Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 0	PCIe channel 0. Transmit Output differential pair.
PCIE_TX0-	A69					
PCIE_RX0+	B68	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 0	PCIe channel 0. Receive Input differential pair.
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 1	PCIe channel 1. Transmit Output differential pair.
PCIE_TX1-	A65					
PCIE_RX1+	B64	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 1	PCIe channel 1. Receive Input differential pair.
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 2	PCIe channel 2. Transmit Output differential pair.
PCIE_TX2-	A62					
PCIE_RX2+	B61	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 2	PCIe channel 2. Receive Input differential pair.
PCIE_RX2-	B62					
PCIE_TX3+	A58	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 3	PCIe channel 3. Transmit Output differential pair.
PCIE_TX3-	A59					
PCIE_RX3+	B58	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 3	PCIe channel 3. Receive Input differential pair.
PCIE_RX3-	B59					
PCIE_TX4+	A55	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 4	PCIe channel 4. Transmit Output differential pair.
PCIE_TX4-	A56					
PCIE_RX4+	B55	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 4	PCIe channel 4. Receive Input differential pair.
PCIE_RX4-	B56					
PCIE_TX5+	A52	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 5	PCIe channel 5. Transmit Output differential pair.
PCIE_TX5-	A53					
PCIE_RX5+	B52	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 5	PCIe channel 5. Receive Input differential pair.
PCIE_RX5-	B53					
PCIE_TX6+	D19	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 6	PCIe channel 6. Transmit Output differential pair.
PCIE_TX6-	D20					
PCIE_RX6+	C19	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 6	PCIe channel 6. Receive Input differential pair.
PCIE_RX6-	C20					
PCIE_TX7+	D22	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Differential Transmit Pairs 7	PCIe channel 7. Transmit Output differential pair.
PCIE_TX7-	D23					
PCIE_RX7+	C22	I PCIE	AC coupled off Module		PCI Express Differential Receive Pairs 7	PCIe channel 7. Receive Input differential pair.
PCIE_RX7-	C23					
PCIE_CLK_REF+	A88	O PCIE	PCIE		Reference clock output for all PCI Express and PCI Express Graphics lanes.	PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes.
PCIE_CLK_REF-	A89					

PEG Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
PEG_TX0+	D52	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 0	PEG channel 0, Transmit Output differential pair.
PEG_TX0-	D53					
PEG_RX0+	C52	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 0	PEG channel 0, Receive Input differential pair.
PEG_RX0-	C53					
PEG_TX1+	D55	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 1	PEG channel 1, Transmit Output differential pair.
PEG_TX1-	D56					
PEG_RX1+	C55	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 1	PEG channel 1, Receive Input differential pair.
PEG_RX1-	C56					
PEG_TX2+	D58	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 2	PEG channel 2, Transmit Output differential pair.
PEG_TX2-	D59					
PEG_RX2+	C58	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 2	PEG channel 2, Receive Input differential pair.
PEG_RX2-	C59					
PEG_TX3+	D61	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 3	PEG channel 3, Transmit Output differential pair.
PEG_TX3-	D62					
PEG_RX3+	C61	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 3	PEG channel 3, Receive Input differential pair.
PEG_RX3-	C62					
PEG_TX4+	D65	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 4	PEG channel 4, Transmit Output differential pair.
PEG_TX4-	D66					
PEG_RX4+	C65	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 4	PEG channel 4, Receive Input differential pair.
PEG_RX4-	C66					
PEG_TX5+	D68	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 5	PEG channel 5, Transmit Output differential pair.
PEG_TX5-	D69					
PEG_RX5+	C68	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 5	PEG channel 5, Receive Input differential pair.
PEG_RX5-	C69					
PEG_TX6+	D71	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 6	PEG channel 6, Transmit Output differential pair.
PEG_TX6-	D72					
PEG_RX6+	C71	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 6	PEG channel 6, Receive Input differential pair.
PEG_RX6-	C72					
PEG_TX7+	D74	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 7	PEG channel 7, Transmit Output differential pair.
PEG_TX7-	D75					
PEG_RX7+	C74	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 7	PEG channel 7, Receive Input differential pair.
PEG_RX7-	C75					
PEG_TX8+	D78	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 8	PEG channel 8, Transmit Output differential pair.
PEG_TX8-	D79					
PEG_RX8+	C78	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 8	PEG channel 8, Receive Input differential pair.
PEG_RX8-	C79					
PEG_TX9+	D81	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 9	PEG channel 9, Transmit Output differential pair.
PEG_TX9-	D82					
PEG_RX9+	C81	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 9	PEG channel 9, Receive Input differential pair.
PEG_RX9-	C82					
PEG_TX10+	D85	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 10	PEG channel 10, Transmit Output differential pair.
PEG_TX10-	D86					

PEG_RX10+	C85	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 10	PEG channel 10, Receive Input differential pair.
PEG_RX10-	C86					
PEG_TX11+	D88	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 11	PEG channel 11, Transmit Output differential pair.
PEG_TX11-	D89					
PEG_RX11+	C88	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 11	PEG channel 11, Receive Input differential pair.
PEG_RX11-	C89					
PEG_TX12+	D91	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 12	PEG channel 12, Transmit Output differential pair.
PEG_TX12-	D92					
PEG_RX12+	C91	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 12	PEG channel 12, Receive Input differential pair.
PEG_RX12-	C92					
PEG_TX13+	D94	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 13	PEG channel 13 Transmit Output differential pair.
PEG_TX13-	D95					
PEG_RX13+	C94	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 13	PEG channel 13, Receive Input differential pair.
PEG_RX13-	C95					
PEG_TX14+	D98	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 14	PEG channel 14, Transmit Output differential pair.
PEG_TX14-	D99					
PEG_RX14+	C98	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 14	PEG channel 14, Receive Input differential pair.
PEG_RX14-	C99					
PEG_TX15+	D101	O PCIE	AC coupled on Module	AC Coupling capacitor	PCI Express Graphics transmit differential pairs 15	PEG channel 15, Transmit Output differential pair.
PEG_TX15-	D102					
PEG_RX15+	C101	I PCIE	AC coupled off Module		PCI Express Graphics receive differential pairs 15	PEG channel 15, Receive Input differential pair.
PEG_RX15-	C102					
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 10KΩ to 3V3	PCI Express Graphics lane reversal input strap. Pull low on the Carrier board to reverse lane order.	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order.

ExpressCard Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
EXCD0_CPPE#	A49	I CMOS	3.3V /3.3V	PU 10k to 3.3V	PCI ExpressCard: PCI Express capable card request, active low, one per card	PCI ExpressCard0: PCI Express capable card request, active low, one per card
EXCD0_PERST#	A48	O CMOS	3.3V /3.3V		PCI ExpressCard: reset, active low, one per card	PCI ExpressCard0: reset, active low, one per card
EXCD1_CPPE#	B48	I CMOS	3.3V /3.3V	PU 10k to 3.3V	PCI ExpressCard: PCI Express capable card request, active low, one percard	PCI ExpressCard1: PCI Express capable card request, active low, one per card
EXCD1_PERST#	B47	O CMOS	3.3V /3.3V		PCI ExpressCard: reset, active low, one per card	PCI ExpressCard1: reset, active low, one per card

USB Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
USB0+	A46	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 0	USB Port 0, data + or D+
USB0-	A45					USB Port 0, data - or D-
USB1+	B46	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 1	USB Port 1, data + or D+
USB1-	B45					USB Port 1, data - or D-
USB2+	A43	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 2	USB Port 2, data + or D+
USB2-	A42					USB Port 2, data - or D-
USB3+	B43	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 3	USB Port 3, data + or D+
USB3-	B42					USB Port 3, data - or D-

USB4+	A40	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 4	USB Port 4, data + or D+
USB4-	A39					USB Port 4, data - or D-
USB5+	B40	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 5	USB Port 5, data + or D+
USB5-	B39					USB Port 5, data - or D-
USB6+	A37	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 6	USB Port 6, data + or D+
USB6-	A36					USB Port 6, data - or D-
USB7+	B37	I/O USB	3.3V Suspend/3.3V		USB differential pairs, channel 7. USB7 may be configured as a USB client or as a host, or both, at the Module designer's discretion. (SH960MD default set as a host)	USB Port 7, data + or D+
USB7-	B36					USB Port 7, data - or D-
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 0 and 1.
USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 2 and 3.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 4 and 5.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10KW to 3.3V Suspend	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.	USB over-current sense, USB ports 6 and 7.
USB_SSTX0+	D4	O PCIE	AC coupled on Module	AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 0, SuperSpeed TX +
USB_SSTX0-	D3					USB Port 0, SuperSpeed TX -
USB_SSRX0+	C4	I PCIE	AC coupled off Module		Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 0, SuperSpeed RX +
USB_SSRX0-	C3					USB Port 0, SuperSpeed RX -
USB_SSTX1+	D7	O PCIE	AC coupled on Module	AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 1, SuperSpeed TX +
USB_SSTX1-	D6					USB Port 1, SuperSpeed TX -
USB_SSRX1+	C7	I PCIE	AC coupled off Module		Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 1, SuperSpeed RX +
USB_SSRX1-	C6					USB Port 1, SuperSpeed RX -
USB_SSTX2+	D10	O PCIE	AC coupled on Module	AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 2, SuperSpeed TX +
USB_SSTX2-	D9					USB Port 2, SuperSpeed TX -
USB_SSRX2+	C10	I PCIE	AC coupled off Module		Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 2, SuperSpeed RX +
USB_SSRX2-	C9					USB Port 2, SuperSpeed RX -
USB_SSTX3+	D13	O PCIE	AC coupled on Module	AC Coupling capacitor	Additional transmit signal differential pairs for the SuperSpeed USB data path.	USB Port 3, SuperSpeed TX +
USB_SSTX3-	D12					USB Port 3, SuperSpeed TX -
USB_SSRX3+	C13	I PCIE	AC coupled off Module		Additional receive signal differential pairs for the SuperSpeed USB data path.	USB Port 3, SuperSpeed RX +
USB_SSRX3-	C12					USB Port 3, SuperSpeed RX -

LVDS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
LVDS_A0+/ eDP_TX2+	A71	O LVDS	LVDS EDP: AC coupled off Module		LVDS Channel A differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board. eDP: eDP differential pairs	LVDS channel A differential signal pair 0 eDP lane 2, TX± differential signal pair
LVDS_A0-/ eDP_TX2-	A72					
LVDS_A1+/ eDP_TX1+	A73	O LVDS	LVDS EDP: AC coupled off Module			LVDS channel A differential signal pair 1 eDP lane 1, TX± differential signal pair
LVDS_A1-/ eDP_TX1-	A74					
LVDS_A2+/ eDP_TX0+	A75	O LVDS	LVDS EDP: AC coupled off Module			LVDS channel A differential signal pair 2 eDP lane 0, TX ± differential signal pair
LVDS_A2-/ eDP_TX0-	A76					
LVDS_A3+	A78	O LVDS	LVDS EDP: AC coupled off Module			LVDS channel A differential signal pair 3
LVDS_A3-	A79					
LVDS_A_CK+/ eDP_TX3+	A81	O LVDS	LVDS		LVDS Channel A differential clock	LVDS channel A differential clock pair eDP lane 3, TX± differential pair
LVDS_A_CK-/ eDP_TX3-	A82					
LVDS_B0+	B71	O LVDS	LVDS		LVDS Channel B differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board.	LVDS channel B differential signal pair 0
LVDS_B0-	B72					
LVDS_B1+	B73	O LVDS	LVDS			LVDS channel B differential signal pair 1
LVDS_B1-	B74					
LVDS_B2+	B75	O LVDS	LVDS			LVDS channel B differential signal pair 2
LVDS_B2-	B76					
LVDS_B3+	B77	O LVDS	LVDS			LVDS channel B differential signal pair 3
LVDS_B3-	B78					
LVDS_B_CK+	B81	O LVDS	LVDS		LVDS Channel B differential clock	LVDS channel B differential clock pair
LVDS_B_CK-	B82					
LVDS_VDD_ EN/eDP_VDD_ EN	A77	O CMOS	3.3V / 3.3V		LVDS panel / eDP power enable	LVDS flat panel power enable. eDP power enable
LVDS_BKLT_ EN/eDP_BKLT_ EN	B79	O CMOS	3.3V / 3.3V		LVDS panel / eDP backlight enable	LVDS flat panel backlight enable high active signal eDP backlight enable
LVDS_BKLT_ CTRL/eDP_ BKLT_CTRL	B83	O CMOS	3.3V / 3.3V	PD 100KW to GND	LVDS panel / eDP backlight brightness control	LVDS flat panel backlight brightness control EDP backlight brightness control
LVDS_I2C_CK/ eDP_AUX+	A83	I/O OD CMOS	3.3V / 3.3V	PU 2.2KW to 3.3V	I2C clock output for LVDS display use / eDP AUX+	DDC I2C clock signal used for flat panel detection and control. eDP auxiliary lane +
LVDS_I2C_ DAT/eDP_AUX-	A84	I/O OD CMOS	3.3V / 3.3V	PU 2.2KW to 3.3V	I2C data line for LVDS display use / eDP AUX-	DDC I2C data signal used for flat panel detection and control. eDP auxiliary lane -
RSVD/eDP_ HPD	A87	I CMOS	3.3V / 3.3V	RSV PD 100KΩ to GND	eDP_HPD:Detection of Hot Plug / Unplug and notification of the link layer	eDP_HPD: Detection of Hot Plug / Unplug and notification of the link layer

LPC Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
LPC_AD0	B4	I/O CMOS	3.3V / 3.3V		LPC multiplexed address, command and data bus.	LPC multiplexed command, address and data.
LPC_AD1	B5					
LPC_AD2	B6					
LPC_AD3	B7					
LPC_FRAME#	B3	O CMOS	3.3V / 3.3V		LPC frame indicates the start of an LPC cycle	LPC frame indicates start of a new cycle or termination of a broken cycle.
LPC_DRQ0#	B8	I CMOS	3.3V / 3.3V	PU 10K to 3.3V, not support.	LPC serial DMA request	LPC encoded DMA/Bus master request.
LPC_DRQ1#	B9			PU 10K to 3.3V, not support.		
LPC_SERIRQ	A50	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V	LPC serial interrupt	LPC serialized IRQ.
LPC_CLK	B10	O CMOS	3.3V / 3.3V	series 22Ω resistor	LPC clock output - 33MHz nominal	LPC clock output 33MHz.

SPI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V		Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1	Chip select for Carrier Board SPI – may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend/3.3V		Data in to Module from Carrier SPI	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend/3.3V		Data out from Module to Carrier SPI	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V		Clock from Module to Carrier SPI	Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend/3.3V		Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board.	Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier.
BIOS_DIS0#	A34	I CMOS	NA	PU 10KΩ to 3V3 Suspend.	Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to COM Express Module Base Specification Revision 2.1 for strapping options of BIOS disable signals.	Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to for strapping options of BIOS disable signals.
BIOS_DIS1#	B88			PU 10KΩ to 3V3 Suspend.		Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low.

VGA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
VGA_RED	B89	O Analog	Analog	PD 150W to GND	Red for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
VGA_GRN	B91	O Analog	Analog	PD 150W to GND	Green for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
VGA_BLU	B92	O Analog	Analog	PD 150W to GND	Blue for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load.	Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load.
VGA_HSYNC	B93	O CMOS	3.3V / 3.3V		Horizontal sync output to VGA monitor	Horizontal sync output to VGA monitor.
VGA_VSYNC	B94	O CMOS	3.3V / 3.3V		Vertical sync output to VGA monitor	Vertical sync output to VGA monitor.
VGA_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PU 2.2KW to 3.3V	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)	DDC clock line (I2C port dedicated to identify VGA monitor capabilities).
VGA_I2C_DAT	B96	I/O OD CMOS	3.3V / 3.3V	PU 2.2KW to 3.3V	DDC data line.	DDC data line.

DDI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
DDI1_PAIR0+	D26	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 0 differential pairs DDI for SDVO: SDVO1_RED± differential pair (Serial Digital Video red output) DDI for HDMI/DVI: TMDS1_DATA lanes 2 differential pairs	DP1_LANE0+ for DP / TMDS1_DATA2+ for HDMI or DVI
DDI1_PAIR0-	D27					DP1_LANE0- for DP / TMDS1_DATA2- for HDMI or DVI
DDI1_PAIR1+	D29	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 1 differential pairs DDI for SDVO: SDVO1_GRN± differential pair (Serial Digital Video green output) DDI for HDMI/DVI: TMDS1_DATA lanes 1 differential pairs	DP1_LANE1+ for DP / TMDS1_DATA1+ for HDMI or DVI
DDI1_PAIR1-	D30					DP1_LANE1- for DP / TMDS1_DATA1- for HDMI or DVI
DDI1_PAIR2+	D32	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 2 differential pairs DDI for SDVO: SDVO1_BLU± differential pair (Serial Digital Video blue output) DDI for HDMI/DVI: TMDS1_DATA lanes 0 differential pairs	DP1_LANE2+ for DP / TMDS1_DATA0+ for HDMI or DVI
DDI1_PAIR2-	D33					DP1_LANE2- for DP / TMDS1_DATA0- for HDMI or DVI
DDI1_PAIR3+	D36	O PCIE	AC coupled off Module		DDI for Display Port: DP1_LANE 3 differential pairs DDI for SDVO: SDVO1_CK± differential pair (Serial Digital Video clock output) DDI for HDMI/DVI: TMDS1_CLK differential pairs	DP1_LANE3+ for DP / TMDS1_CLK+
DDI1_PAIR3-	D37					DP1_LANE3- for DP / TMDS1_CLK-
DDI1_PAIR4+	C25	I PCIE	AC coupled off Module	NC	DDI for SDVO: SDVO1_INT± differential pair (Serial Digital Video B interrupt input differential pair)	NA
DDI1_PAIR4-	C26			NC		NA
DDI1_PAIR5+	C29	I PCIE	AC coupled off Module	NC	DDI for SDVO: SDVO1_TVCLKIN± differential pair (Serial Digital Video TVOUT synchronization clock input differential pair.)	NA
DDI1_PAIR5-	C30			NC		NA
DDI1_PAIR6+	C15	I PCIE	AC coupled off Module	NC	DDI for SDVO: SDVO1_FLDSTALL± differential pair (Serial Digital Video Field Stall input differential pair.)	NA
DDI1_PAIR6-	C16			NC		NA
DDI1_ CTRLCLK_ AUX+	D15	I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	DDI for Display Port: DP1_AUX+ Differetial pairs (DP AUX+ function if DDI1_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP1_AUX+ for DP
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd resistor)	DDI for SDVO: SDVO1_CTRLCLK (SDVO I2C clock line - to set up SDVO peripherals.) DDI for HDMI/DVI: HDMI1_CTRLCLK (HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high)	HDMI1_CTRLCLK for HDMI or DVI
DDI1_ CTRLCLK_ AUX-	D16	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	DDI for Display Port: DP1_AUX- Differetial pairs (DP AUX- function if DDI1_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP1_AUX- for DP
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V (S/W IC between 2.2K/100K resistor)	DDI for SDVO: SDVO1_CTRLDATA (SDVO I2C data line - to set up SDVO peripherals.) DDI for HDMI/DVI: HDMI1_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high)	HDMI1_CTRLDATA for HDMI or DVI
DDI1_HPD	C24	I CMOS	3.3V / 3.3V	PD 1M to GND	DDI for Display Port: DP1_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI1_HPD (HDMI Hot-Plug Detect)	DP1_HPD for DP / HDMI1_HPD for HDMI or DVI
DDI1_DDC_ AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Selects the function of DP1 AUX±(Low) or HDMI1 DDC CLK/DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.

DDI2_PAIR0+	D39	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 0 differential pairs DDI for HDMI/DVI: TMDS2_DATA lanes 2 differential pairs	DP2_LANE0+ for DP / TMDS2_DATA2+ for HDMI or DVI
DDI2_PAIR0-	D40					DP2_LANE0- for DP / TMDS2_DATA2- for HDMI or DVI
DDI2_PAIR1+	D42	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 1 differential pairs DDI for HDMI/DVI: TMDS2_DATA lanes 1 differential pairs	DP2_LANE1+ for DP / TMDS2_DATA1+ for HDMI or DVI
DDI2_PAIR1-	D43					DP2_LANE1- for DP / TMDS2_DATA1- for HDMI or DVI
DDI2_PAIR2+	D46	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 2 differential pairs DDI for HDMI/DVI: TMDS2_DATA lanes 0 differential pairs	DP2_LANE2+ for DP / TMDS2_DATA0+ for HDMI or DVI
DDI2_PAIR2-	D47					DP2_LANE2- for DP / TMDS2_DATA0- for HDMI or DVI
DDI2_PAIR3+	D49	O PCIE	AC coupled off Module		DDI for Display Port: DP2_LANE 3 differential pairs DDI for HDMI/DVI: TMDS2_CLK differential pairs	DP2_LANE3+ for DP / TMDS2_CLK+
DDI2_PAIR3-	D50					DP2_LANE3- for DP / TMDS2_CLK-
DDI2_ CTRLCLK_ AUX+	C32	I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	DDI for Display Port: DP2_AUX+ Differetial pairs (DP AUX+ function if DDI2_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP2_AUX+ for DP
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd resistor)	DDI for HDMI/DVI: HDMI2_CTRLCLK (HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high)	HDMI2_CTRLCLK for HDMI or DVI
DDI2_ CTRLCLK_ AUX-	C33	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	DDI for Display Port: DP2_AUX- Differetial pairs (DP AUX- function if DDI2_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP2_AUX- for DP
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V (S/W IC between 2.2K/100K resistor)	DDI for HDMI/DVI: HDMI2_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high)	HDMI2_CTRLDATA for HDMI or DVI
DDI2_HPD	D44	I CMOS	3.3V / 3.3V	PD 1M to GND	DDI for Display Port: DP2_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI2_HPD (HDMI Hot-Plug Detect)	DP2_HPD for DP / HDMI1_HPD for HDMI or DVI
DDI2_DDC_ AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Selects the function of DP2 AUX±(Low) or HDMI2 DDC CLK/DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.
DDI3_PAIR0+	C39	O PCIE	AC coupled off Module		DDI for Display Port: DP3_LANE 0 differential pairs DDI for HDMI/DVI: TMDS3_DATA lanes 2 differential pairs	DP3_LANE0+ for DP / TMDS3_DATA2+ for HDMI or DVI
DDI3_PAIR0-	C40					DP3_LANE0- for DP / TMDS3_DATA2- for HDMI or DVI
DDI3_PAIR1+	C42	O PCIE	AC coupled off Module		DDI for Display Port: DP3_LANE 1 differential pairs DDI for HDMI/DVI: TMDS3_DATA lanes 1 differential pairs	DP3_LANE1+ for DP / TMDS3_DATA1+ for HDMI or DVI
DDI3_PAIR1-	C43					DP3_LANE1- for DP / TMDS3_DATA1- for HDMI or DVI
DDI3_PAIR2+	C46	O PCIE	AC coupled off Module		DDI for Display Port: DP3_LANE 2 differential pairs DDI for HDMI/DVI: TMDS3_DATA lanes 0 differential pairs	DP3_LANE2+ for DP / TMDS3_DATA0+ for HDMI or DVI
DDI3_PAIR2-	C47					DP3_LANE2- for DP / TMDS3_DATA0- for HDMI or DVI

DDI3_PAIR3+	C49	O PCIE	AC coupled off Module		DDI for Display Port: DP3_LANE 3 differential pairs DDI for HDMI/DVI: TMDS3_CLK differential pairs	DP3_LANE3+ for DP / TMDS3_CLK+
DDI3_PAIR3-	C50					DP3_LANE3- for DP / TMDS3_CLK-
DDI3_ CTRLCLK_ AUX+	C36	I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	DDI for Display Port: DP3_AUX+ Differetial pairs (DP AUX+ function if DDI3_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access	DP3_AUX+ for DP
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd resistor)	DDI for HDMI/DVI: HDMI3_CTRLCLK (HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high)	HDMI3_CTRLCLK for HDMI or DVI
DDI3_ CTRLCLK_ AUX-	C37	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	DDI for Display Port: DP3_AUX- Differetial pairs (DP AUX- function if DDI3_DDC_AUX_SEL is no connect)	DP3_AUX- for DP
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V (S/W IC between 2.2K/100K resistor)	DDI for HDMI/DVI: HDMI3_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high)	HDMI3_CTRLDATA for HDMI or DVI
DDI3_HPD	C44	I CMOS	3.3V / 3.3V	PD 1MΩ to GND	DDI for Display Port: DP3_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI3_HPD (HDMI Hot-Plug Detect)	DP3_HPD for DP / HDMI1_HPD for HDMI or DVI
DDI3_DDC_ AUX_SEL	C38	I CMOS	3.3V / 3.3V	PD 1MΩ to GND	Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals.	Selects the function of DP3 AUX±(Low) or HDMI3 DDC CLK/DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels.

Serial Interface Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
SER0_TX	A98	O CMOS	5V/12V		General purpose serial port 0 transmitter	Transmit Line for Serial Port 0 ; PD 4.7KΩ
SER0_RX	A99	I CMOS	5V/12V	PU 10KΩ to 3.3V	General purpose serial port 0 receiver	Receive Line for Serial Port 0
SER1_TX	A101	O CMOS	5V/12V		General purpose serial port 1 transmitter	Transmit Line for Serial Port 1 ; PD 4.7KΩ
SER1_RX	A102	I CMOS	5V/12V	PU 10KΩ to 3.3V	General purpose serial port 1 receiver	Receive Line for Serial Port 1

I2C Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3V Suspend	General purpose I2C port clock output	General Purpose I2C Clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3V Suspend	General purpose I2C port data I/O line	General Purpose I2C data I/O line.

Miscellaneous Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
SPKR	B32	O CMOS	3.3V / 3.3V		Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.	Output used to control an external FET or a logic gate to drive an external PC speaker.
WDT	B27	O CMOS	3.3V / 3.3V		Output indicating that a watchdog time-out event has occurred.	Output indicating that a watchdog time-out event has occurred.
FAN_PWNOUT	B101	O CMOS	3.3V / 12V	RSV PD 100KΩ to GND	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.	Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.
FAN_TACHIN	B102	I OD CMOS	3.3V / 12V	PU 47KΩ to 3.3V	Fan tachometer input for a fan with a two pulse output.	Fan tachometer input for a fan with a two pulse output.
TPM_PP	A96	I CMOS	3.3V / 3.3V	PD 100KΩ to GND.	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM.	Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. Thissignal is used to indicate Physical Presence to the TPM.

Power and System Management Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.	Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.	Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V	PD 100KΩ to GND	Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.	Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board.
PWR_OK	B24	I CMOS	3.3V / 3.3V	PU 10KΩ to 3.3V	Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.	Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation.
SUS_STAT#	B18	O CMOS	3.3V Suspend/3.3V		Indicates imminent suspend operation; used to notify LPC devices.	Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V	PD 100KΩ to GND	Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.	S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM).
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V	PD 100KΩ to GND	Indicates system is in Suspend to Disk state. Active low output.	S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk).
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V	PD 100KΩ to GND	Indicates system is in Soft Off state.	S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off).
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 10KΩ to 3.3V Suspend	PCI Express wake up signal.	PCI Express wake-up event signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	Integrate PU @PCH	General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.	General purpose wake-up signal.

BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10KΩ to 3.3V Suspend	Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	LID switch. Low active signal used by the ACPI operating system for a LID switch.	LID switch. Low active signal used by the ACPI operating system for a LID switch.
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 47KΩ to 3.3V Suspend	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.	Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.

Thermal Protection Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
THRM#	B35	I CMOS	3.3V / 3.3V	PU 10KΩ to 3.3V	Input from off-Module temp sensor indicating an over-temp situation.	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10KΩ to 3.3V	Active low output indicating that the CPU has entered thermal shutdown.	Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off).

SMBUS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional clock line.	System Management Bus bidirectional clock line
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	System Management Bus bidirectional data line.	System Management bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 2.2KΩ to 3.3V Suspend	System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.	System Management Bus Alert

GPIO Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
GPO0	A93	O CMOS	3.3V / 3.3V		General purpose output pins. Upon a hardware reset, these outputs should be low.	General Purpose Outputs for system specific usage.
GPO1	B54					
GPO2	B57					
GPO3	B63					
GPI0	A54	I CMOS	3.3V / 3.3V	PU 47KΩ to 3.3V	General purpose input pins. Pulled high internally on the Module.	General Purpose Input for system specific usage. The signals are pulled up by the Module.
GPI1	A63			PU 47KΩ to 3.3V		
GPI2	A67			PU 47KΩ to 3.3V		
GPI3	A85			PU 47KΩ to 3.3V		

Power and GND Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
VCC_12V	A104~A109 B104~B109 C104~C109 D104~D109	Power			Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.	
VCC_5V_SBY	B84~B87	Power			Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.	
VCC_RTC	A47	Power			Real-time clock circuit-power input. Nominally +3.0V.	
GND	Pin Type = Power. Pin#: A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41,D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.	

Module type Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	SH960MD PU/PD	Module Base Specification R2.1 Description	COM Express Carrier Design Guide R2.0 Description
TYPE0#	C54	PDS		N.C.	TYPE2# TYPE1# TYPE0# X X X pin out Type 1 NC NC NC pin out Type 2 NC NC GND pin out Type 3 (no IDE) NC GND NC pin out Type 4 (no PCI) NC GND GND pin out Type 5 (no IDE, no PCI) GND NC NC pin out Type 6 (no IDE, no PCI)	The Type pins indicate the COM Express pin-out type of the Module. To indicate the Module's pin-out type, the pins are either not connected or strapped to ground on the Module. The Carrier Board has to implement additional logic, which prevents the system to switch power on, if a Module with an incompatible pin-out type is detected.
TYPE1#	C57	PDS		N.C.		
TYPE2#	D57	PDS		PD 0Ω to GND		
TYPE10#	A97	PDS		N.C.	Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0/2.0 Module is installed TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47K resistor 12V Pin-out R1.0 This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. Type 10 Modules shall pull this pin to ground through a 47K resistor.	Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 1.0/2.0 Module is installed. TYPE10# NC Pin-out R2.0 PD Pin-out Type 10 pull down to ground with 47k 12V Pin-out R1.0

Chapter 3 - BIOS Setup

▶ Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.
It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration
Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility
The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.
The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

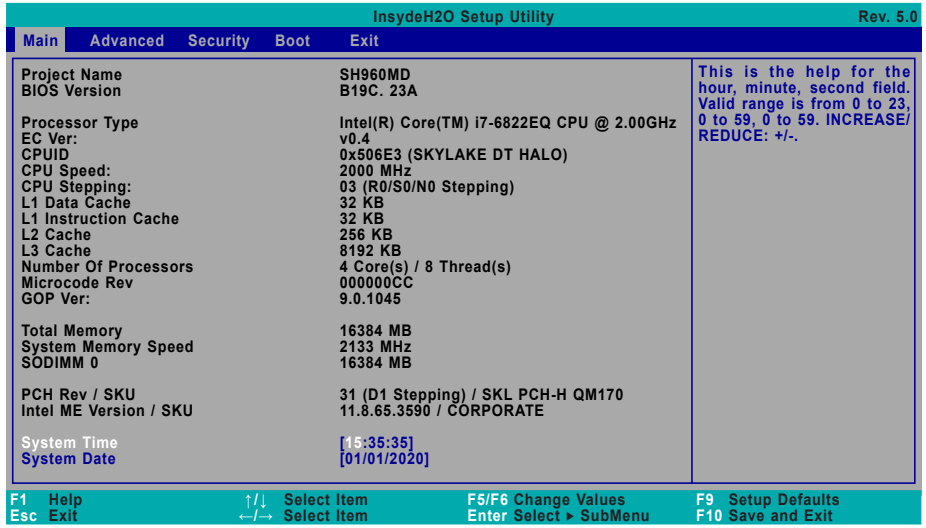
Keys	Function
Right / Left arrow	Move the highlight left or right to select a menu
Up / Down arrow	Move the highlight up or down between submenus or fields
<Enter>	Enter the highlighted submenu
+ (plus key)/F6	Scroll forward through the values or options of the highlighted field
- (minus key)/F5	Scroll backward through the values or options of the highlighted field
<F1>	Display general help
<F9>	Optimized defaults
<F10>	Save and Exit
<Esc>	Return to previous menu

Scroll Bar
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu
When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

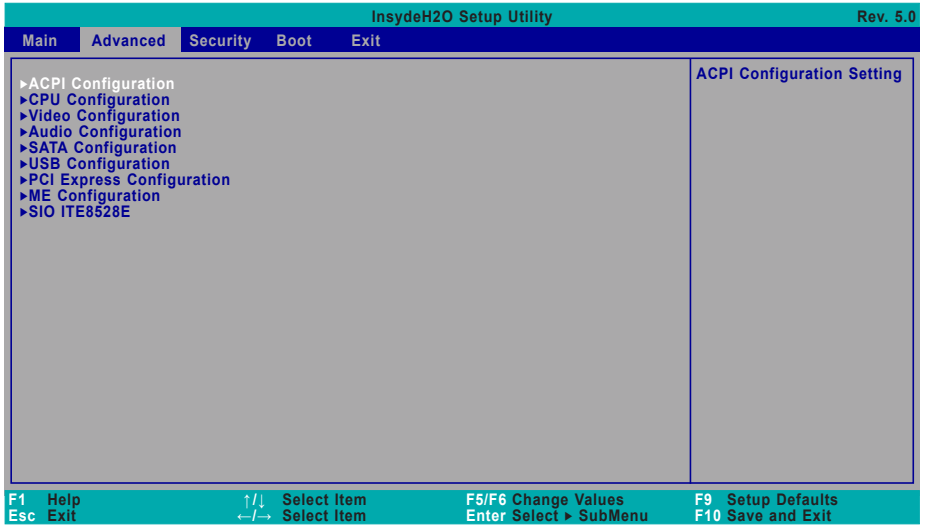
System Date

The date format is <month>, <date>, <year>. Month displays the month, from 01 to 12. Date displays the date, from 01 to 31. Year displays the year, from 2000 to 2099.

▶ Advanced

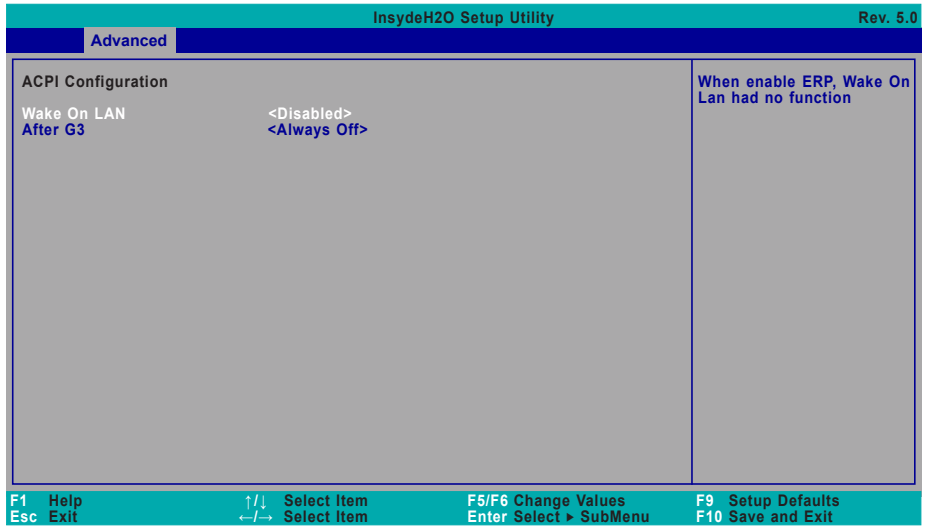
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



▶ Advanced

ACPI Configuration



Wake On LAN

Enable or Disable this field to allow LAN signal to power up the system.

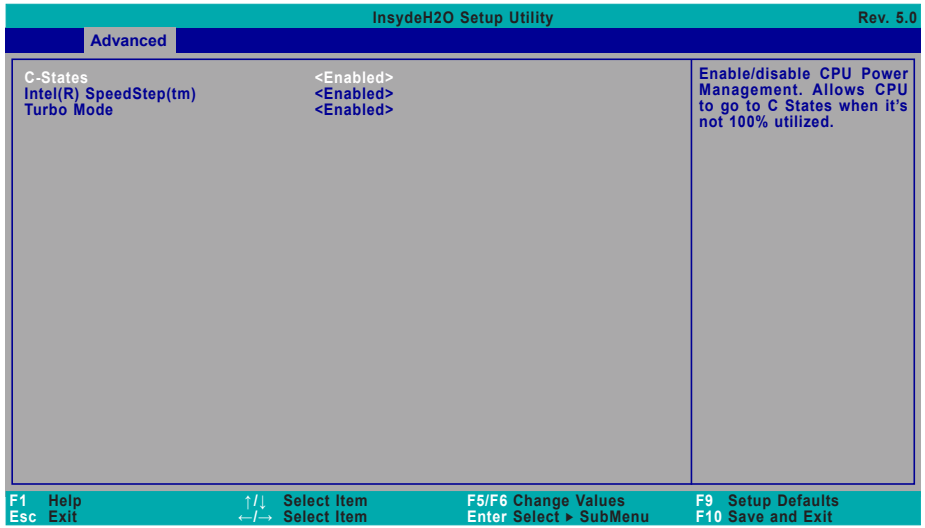
After G3

Select between S0 State, Last State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

S0 State	The system automatically powers on after power failure.
S5 State	The system enter soft-off state after power failure. Power-on signal input is required to power up the system.

▶ Advanced

CPU Configuration



C-States

Enable or disable CPU Power Management. It allows CPU to go to C States when it's not 100% utilized.

Intel(R) SpeedStep(tm)

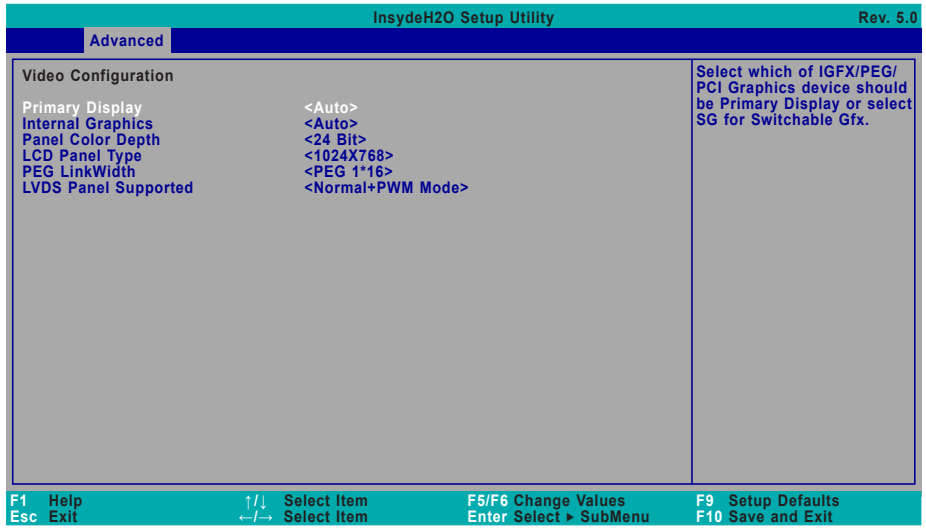
This field is used to enable or disable the Enhanced Intel SpeedStep® Technology (EIST), which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, EIST features can then be enabled via the operating system's power management.

Turbo Mode

Enable or disable turbo mode of the processor. This field will only be displayed when EIST is enabled.

▶ Advanced

Video Configuration



Primary Display

Select either IGFX, PEG, or PCIe Graphics device to be the primary display.

Internal Graphics

Keep IGFX enabled or disabled based on the setup options.

LCD Panel Color Depth

Select the LCD panel color depth — 18 Bit, 24 Bit, 36 Bit or 48 Bit.

LCD Panel Type

Please check the specifications of your LCD monitor. Select the type of LCD panel connected to the system's LCD connector — 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1920X1080 or 1920X1200.

PEG LinkWidth

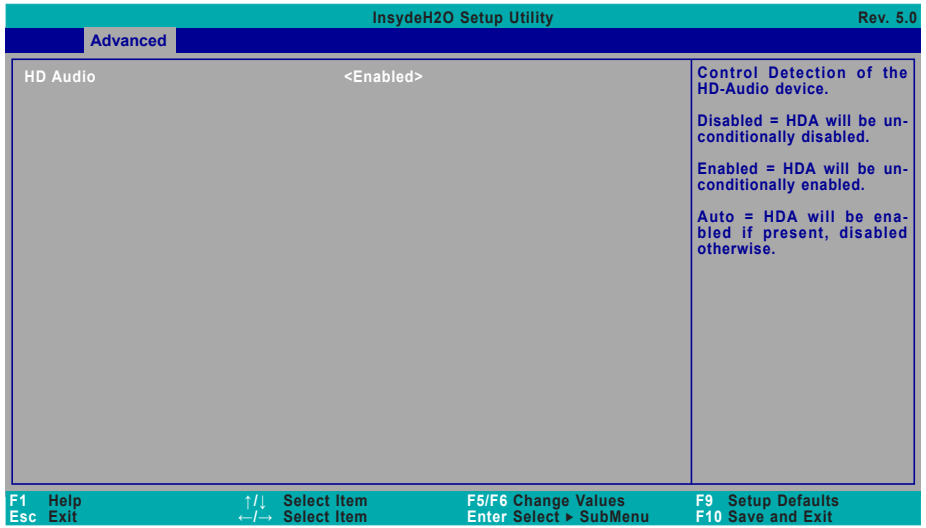
Configure the PEG's lane bandwidth and numbers — 1*8 and 2*4, 2*8, or 1*16.

LVDS Panel Supported

Enable or disable PTN3460's function to support LVDS panel.

▶ Advanced

Audio Configuration



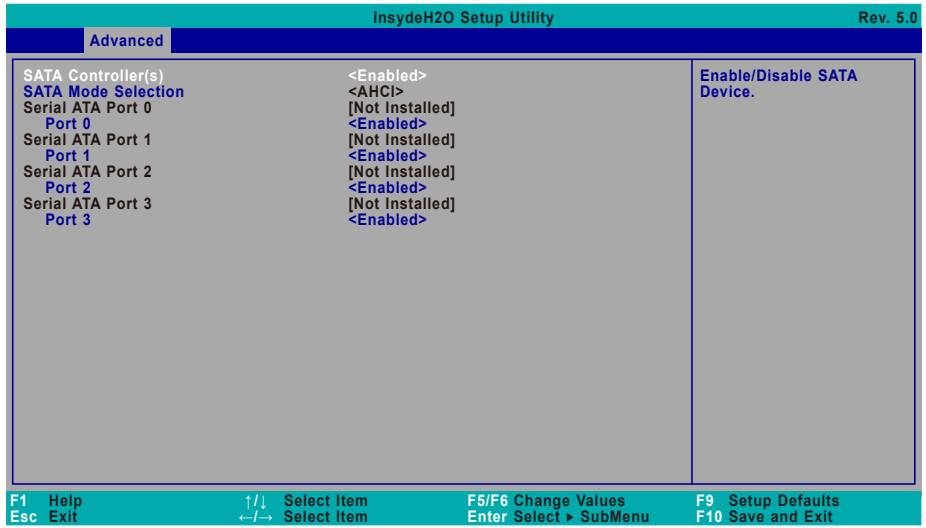
HD Audio

Enable or disable HD audio support.

Disabled	HD Audio will be disabled.
Enabled	HD Audio will be enabled.

▶ Advanced

SATA Configuration



SATA Controller(s)

Enable or disable the Serial ATA controller. This following fields will only be displayed when this field is enabled.

SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

AHCI This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

RAID This option allows you to create RAID or Intel Rapid Storage configuration.

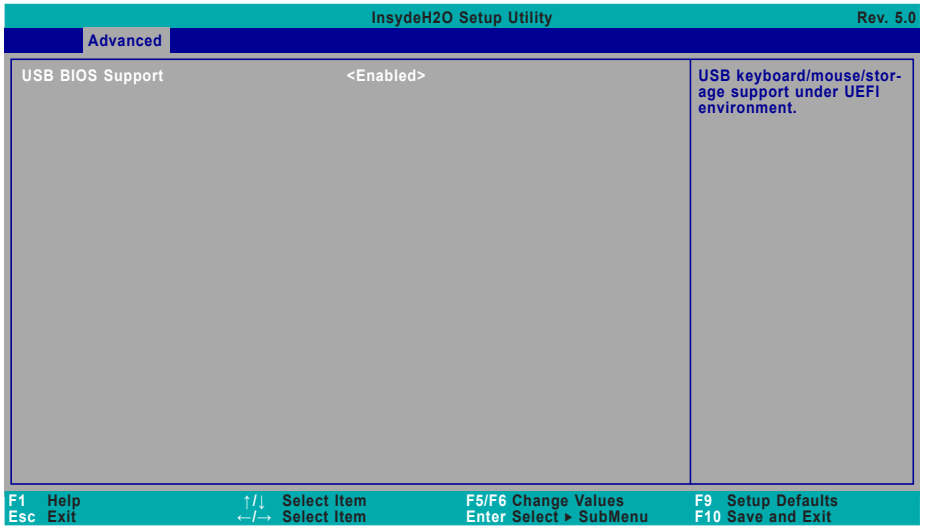
SATA Port 0

Enable or disable each Serial ATA port.

Note:
The devices shown here are based on a carrier board that may not resemble your actual carrier board. The actual I/O devices depend entirely on those present on your actual carrier board.

▶ Advanced

USB Configuration

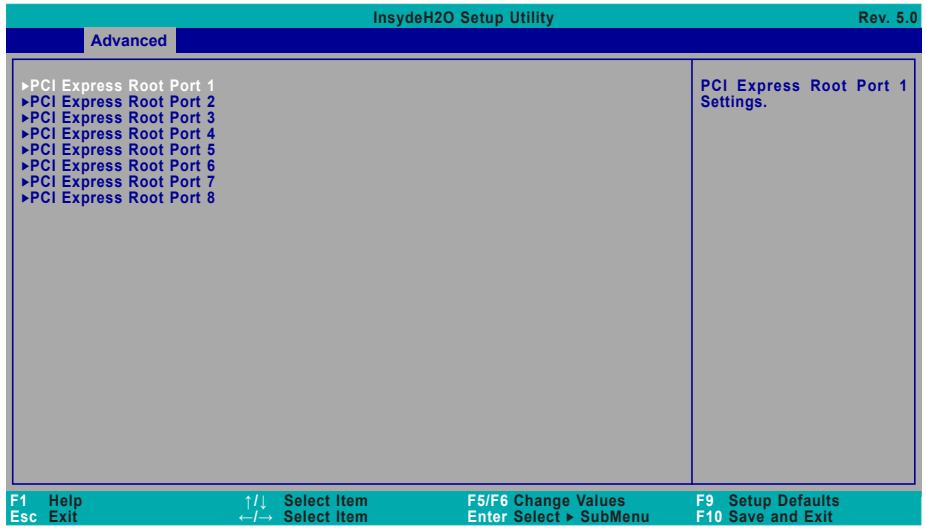


USB BIOS Support

Enable or disable the USB devices such as keyboard, mouse, and storage devices under UEFI environment.

▶ Advanced

PCI Express Configuration



▶ PCI Express Root Port 1/2/3/4/5/6/7/8

Press Enter to enter the sub-menu of the selected port.

PCI Express Root Port 1/2/3/4/5/6/7/8

Enable or disable the selected port.

PCIe Speed

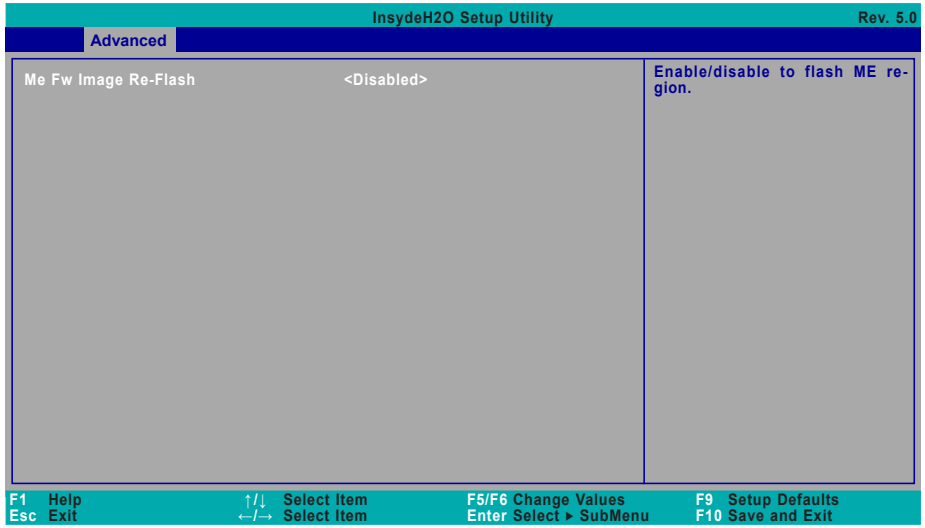
Select PCIe Speed of the current port — AUTO, Gen1, Gen2, or Gen3. Gen 3 is only available for the PCIE1 port. This field may not appear when the speed of the port is not configurable.

Note:
The devices shown here are based on a carrier board that may not resemble your actual carrier board. The actual I/O devices depend entirely on those present on your actual carrier board.

▶ Advanced

ME Configuration

Configure Management Engine related settings in this page.

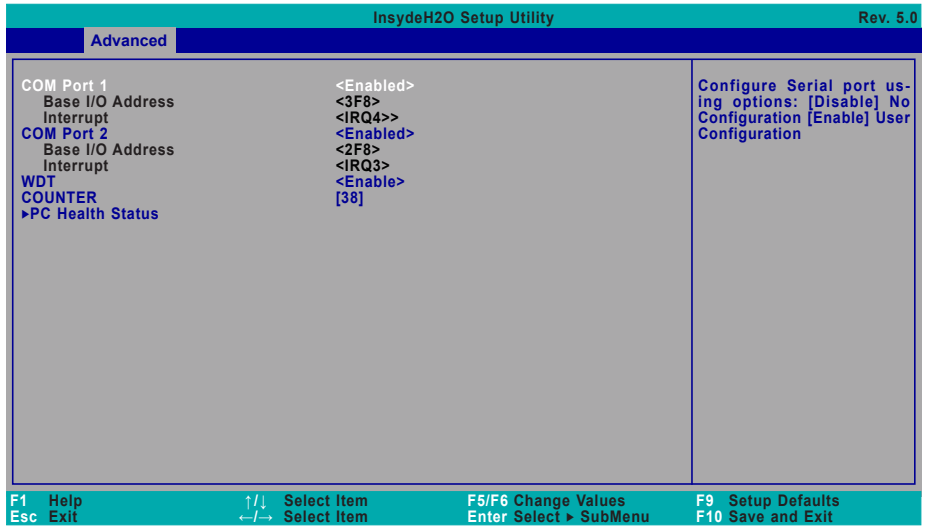


Me Fw Image Re-Flash

Enabled	Allow the user to re-write the ME firmware.
Disabled	ME firmware re-write is not allowed.

▶ Advanced

SIO ITE8528E



Super I/O are additional monitoring and controlling functions over certain I/O ports.

COM Port 1-2

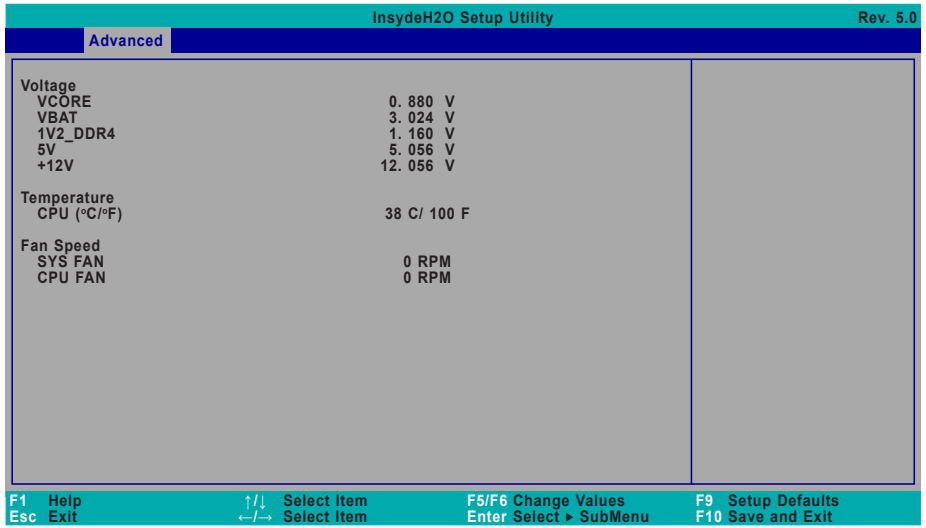
Enable or disable user-defined parameters.

WDT

Enable or disable the watchdog function. When enabled, a time-out counter field ranging from 1 to 255 seconds will be displayed. Press Enter and input valid numerals, and press Enter again to select from [Yes] to save or [No] to abort.

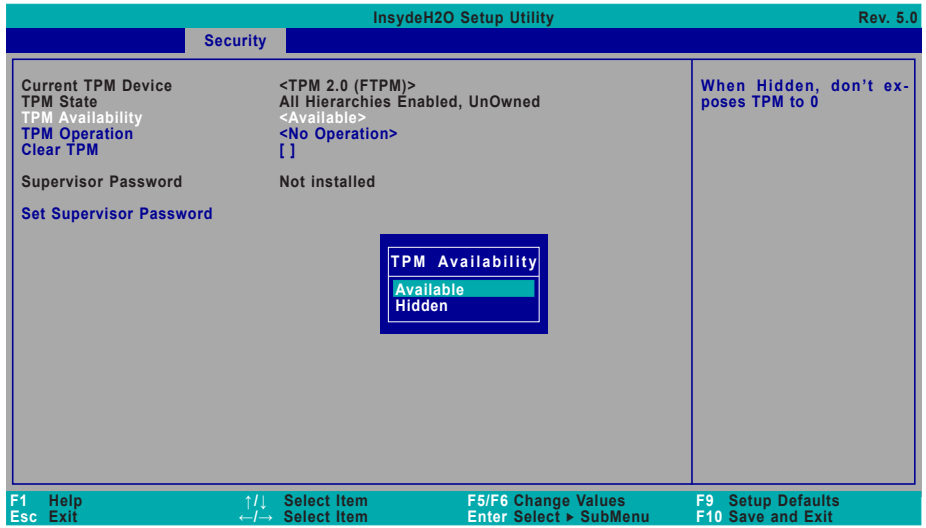
Note:
The devices shown here are based on a carrier board that may not resemble your actual carrier board. The actual I/O devices depend entirely on those present on your actual carrier board.

▶ PC Health Status



This section displays the system's health information, i.e. voltage readings, CPU and system temperatures, and fan speed readings.

▶ Security



TPM Availability

Show or hide the TPM availability and its configurations.

TPM Operation

Select one of the supported operation to change TPM2 state.

Clear TPM

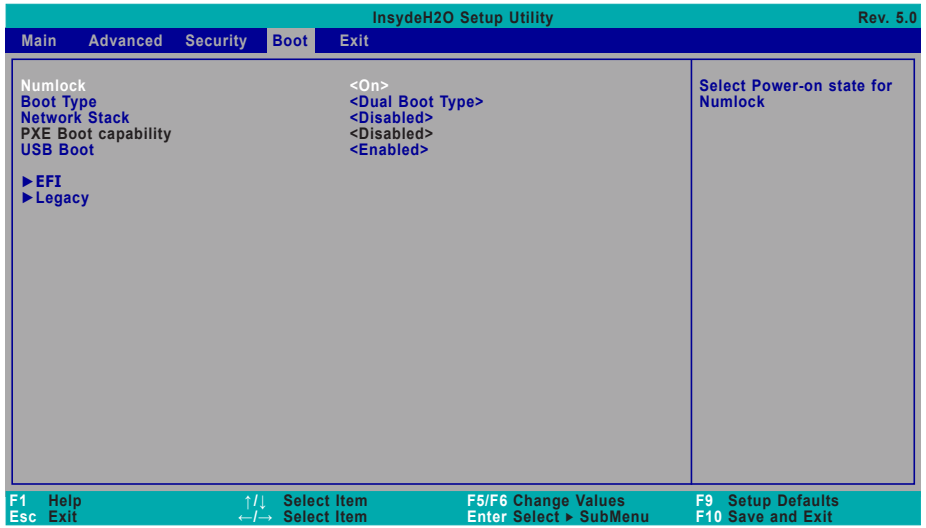
Remove all TPM context associated with a specific Owner.

Set Supervisor Password

Set the supervisor's password and the length of the password must be greater than one character.

Note:
The devices shown here are based on a carrier board that may not resemble your actual carrier board. The actual I/O devices depend entirely on those present on your actual carrier board.

▶ Boot



Numlock

Select the power-on state for numlock.

Boot Type

Select the boot type — UEFI Boot Type, Legacy Boot Type or Dual Boot Type. If you select "UEFI Boot Type" or "Dual Boot Type", the "Network Stack", "PXE Boot capability", "USB Boot" and "Quiet Boot" will show up. If you select "Legacy Boot Type", "PXE Boot to LAN", "USB Boot" and "Quiet Boot" will show up.

Note:
Please press F10 to save the settings and re-start the system board after changing "Boot Type".

Network Stack

This field is used to enable or disable network stacks, i.e. IPv4 or IPv6 network protocols.

PXE Boot capability

This field is only available when "Boot Type" is set to “UEFI Boot Type” or “Dual Boot Type”, and when "Network Stack" is enabled.

Disabled Suppoort Network Stack
UEFI IPv4/IPv6
Legacy Legacy PXE OPROM only

PXE Boot to LAN

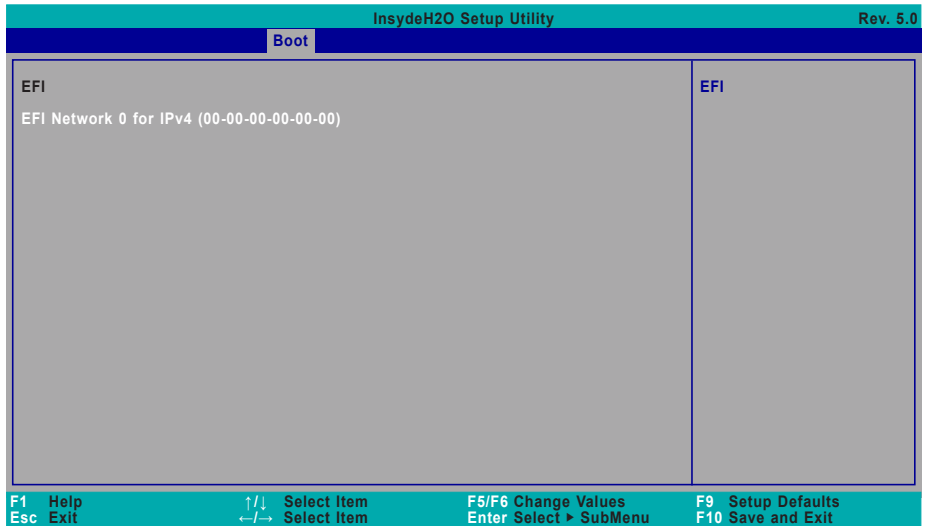
Enable or disable Boot into the Pre-boot Execution Environment (PXE) stored in the LAN. This field is only available when "Boot Type" is set to “Legacy Boot Type” or “Dual Boot Type”, and when "Network Stack" is enabled.

USB Boot

Enable or disable booting to USB boot devices.

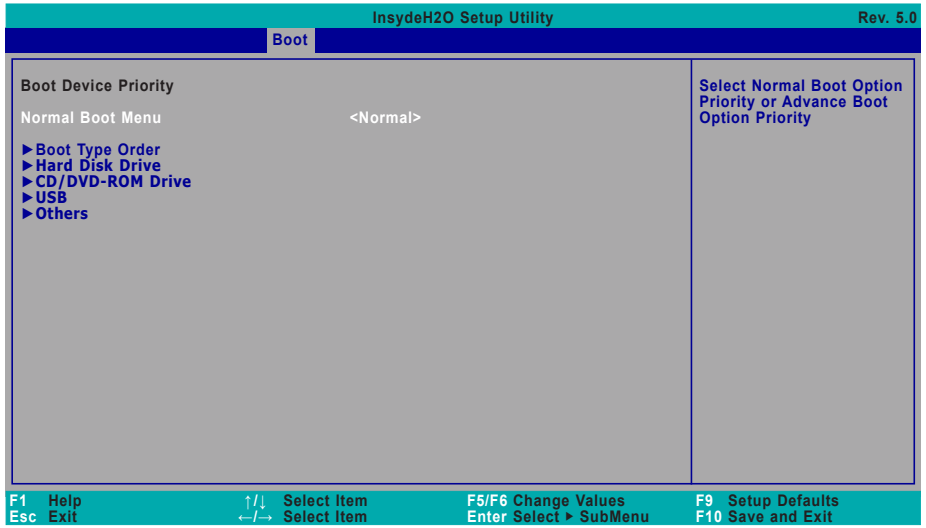
▶ EFI

Configure boot priorities in this submenu. Press -/+ or F5/F6 to move the highlighted item down/up the priority list. This field is only available when "Boot Type" is set to “UEFI Boot Type” or "Dual Boot Type".



▶ Legacy

Configure boot priorities in this submenu. Re-arrange the order by pressing -/+ or F5/F6 to move the highlighted item down/up the priority list. This field is only available when "Boot Type" is set to “Legacy Boot Type” or "Dual Boot Type".



Normal Boot Menu

Select a priority arranging method.

Normal Boot priority is arranged according to the type of the storage devices, and the configured order.
Advance Boot priority is arranged according to the configured order regardless of the type of the storage devices.

▶Boot Type Order

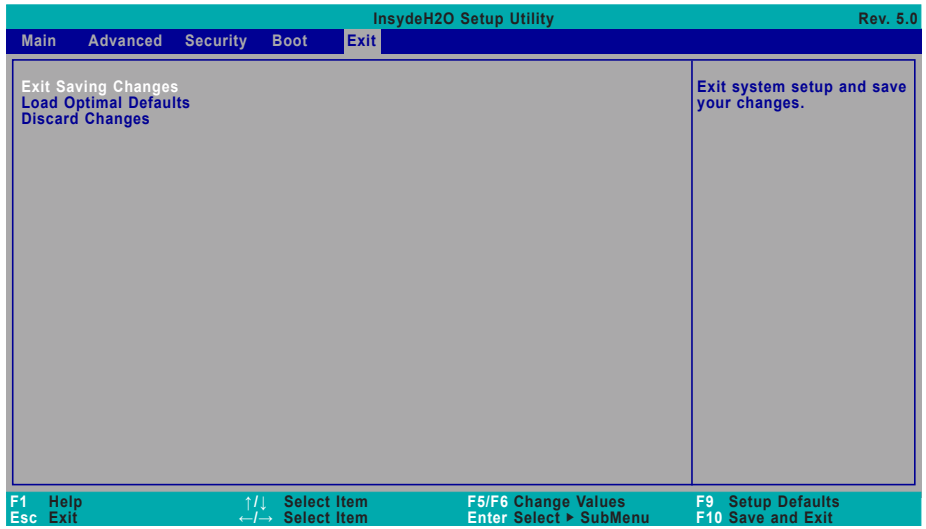
Arrange the priority of types of the storage devices.

▶Hard Disk Drive/ ▶CD/DVD-ROM Drive / ▶USB / ▶Others

Arrange the priority of the storage devices in each category. The submenu will not be displayed when there is no available storage device of the type.

Note:
When a desired LAN port for PXE boot is not listed as a boot device, please confirm that the "PXE Boot to LAN", "PXE boot capability", "Network Stack" and the LAN controller of the said LAN (go to "Advanced" > "PCI Express Configuration") are enabled. Please press F10 to save the settings and re-start the system board for the settings to take effect.

▶ Exit



Exit Saving Changes

Select Yes and press <Enter> to exit the system setup and save your changes.

Load Optimal Defaults

Select YES and press <Enter> to load optimal defaults.

Discard Changes

Select YES and press <Enter> to exit the system setup without saving your changes.

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility. For updating Insyde BIOS in UEFI mode, you may refer to the how-to video at https://www.dfi.com/tw/knowledge/video/31.

▶ Notice: BIOS SPI ROM

1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:

a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.

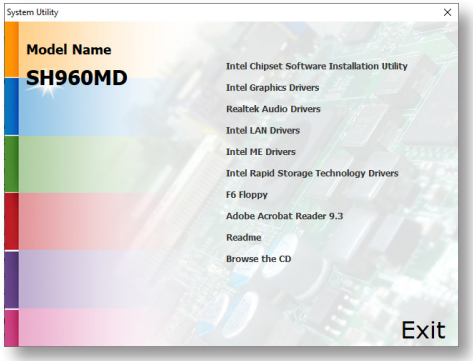
b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

Chapter 4 - Supported Software

Install drivers, utilities and software applications that are required to facilitate and enhance the performance of the system board. You may acquire the software from your sales representatives, from a DVD included in the shipment, or from the website download page at https://www.dfi.com/DownloadCenter.

▶ Auto-run Menu

After inserting your DVD-ROM into your optical drive or executing your DVD image, the System Utility auto-run menu may pop up. Click on the utility or driver that is to be installed on the system. Please refer to the following sections that correspond to your selection for more information.

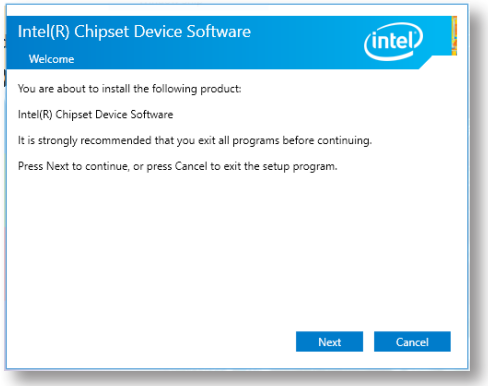


Note:
This step can be ignored if the applications are standalone files.

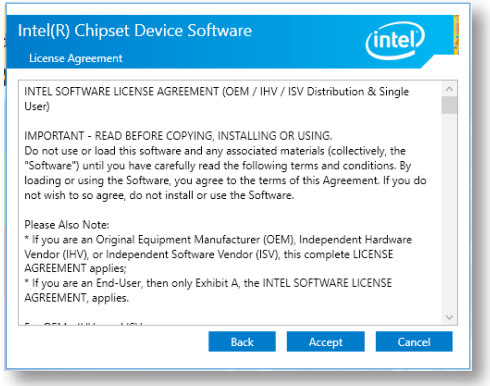
▶ Intel Chipset Software Installation Utility

The Intel Chipset Software Installation Utility is used for updating Windows® INF files so that the Intel chipset can be recognized and configured properly in the system.

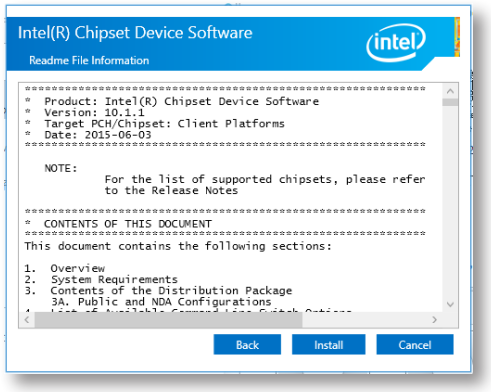
1. Setup is ready to install the utility. Click "Next".



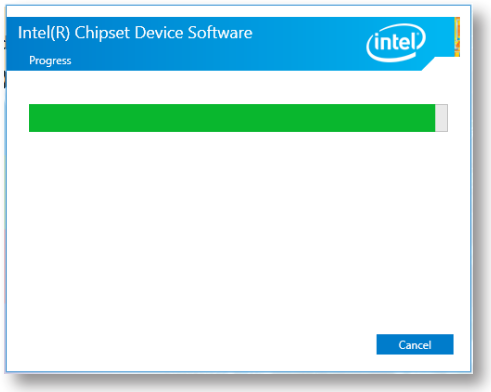
2. Read the license agreement then click "Accept".



3. Go through the readme document for more installation tips then click “Install”.

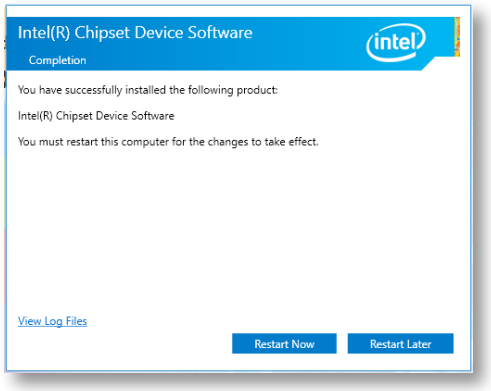


4. The step displays the installing status in the progress.



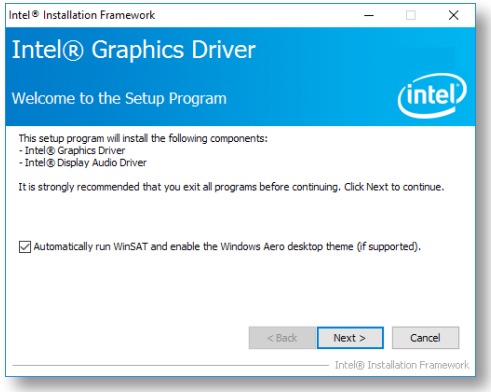
5. After completing installation, click “Restart Now” to exit setup.

   Restarting the system will allow the new software installation to take effect.



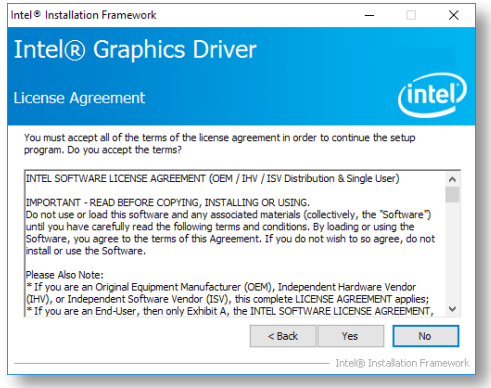
▶ Intel HD Graphics Drivers

1. Setup is now ready to install the graphics driver. Click “Next”.

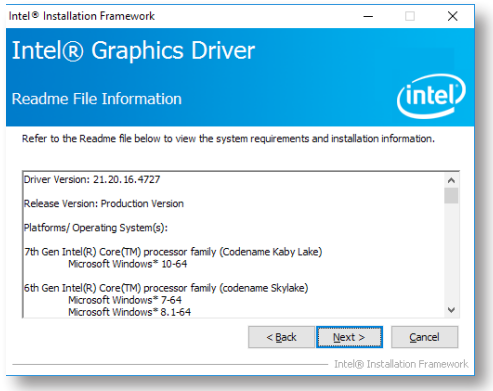


By default, the “Automatically run WinSAT and enable the Windows Aero desktop theme” is enabled. With this enabled, after installing the graphics driver and the system rebooted, the screen will turn blank for 1 to 2 minutes (while WinSAT is running) before the Windows 10 desktop appears. The “blank screen” period is the time Windows is testing the graphics performance.
We recommend that you skip this process by disabling this function then click “Next”.

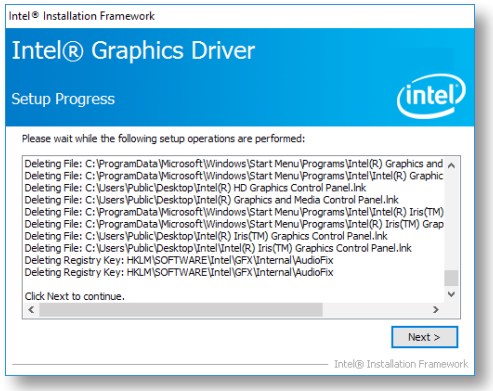
2. Read the license agreement then click “Yes”.



3. Go through the readme document for system requirements and installation tips then click “Next”.

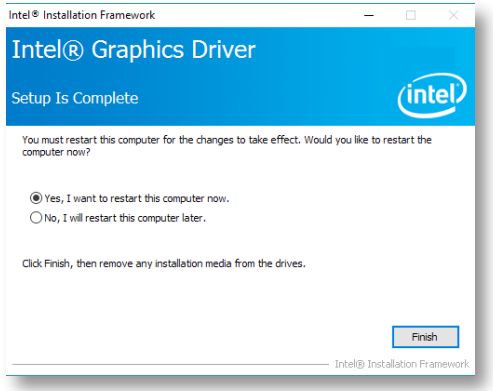


4. Setup is now installing the driver. Click “Next” to continue.



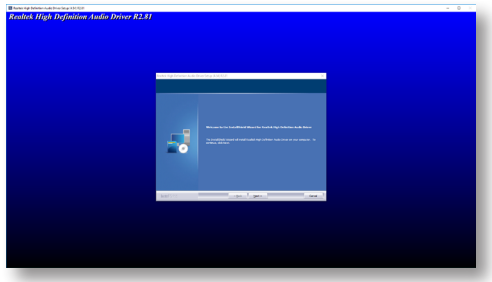
5. Click “Yes, I want to restart this computer now” then click “Finish”.

   Restarting the system will allow the new software installation to take effect.



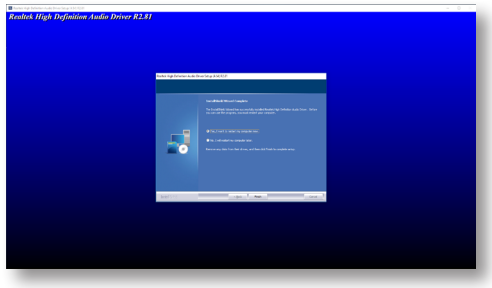
▶ Realtek Audio Drivers

1. Setup is ready to install the driver. Click “Next”.



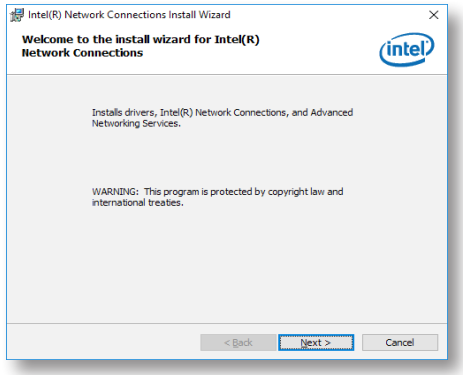
2. Click “Yes, I want to restart my computer now” then click “Finish”.

   Restarting the system will allow the new software installation to take effect.

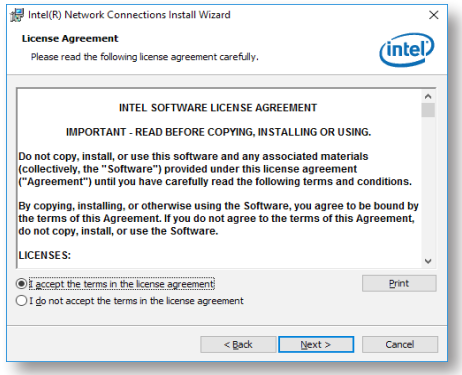


▶ Intel LAN Driver

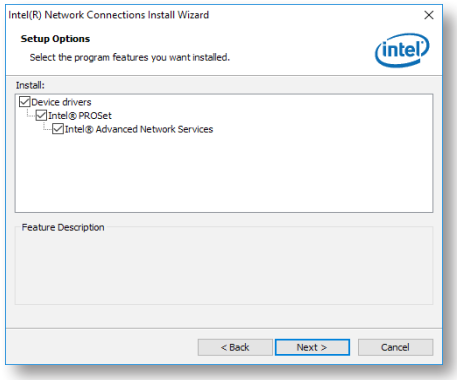
1. Setup is ready to install the driver. Click “Next”.



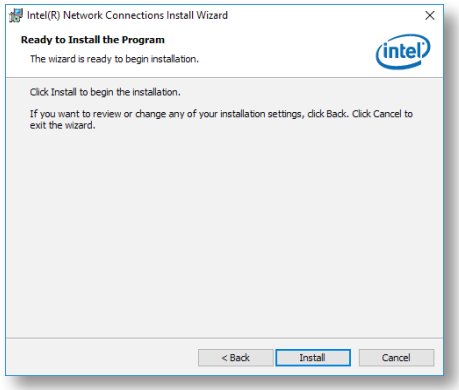
2. Click “I accept the terms in the license agreement” then click “Next”.



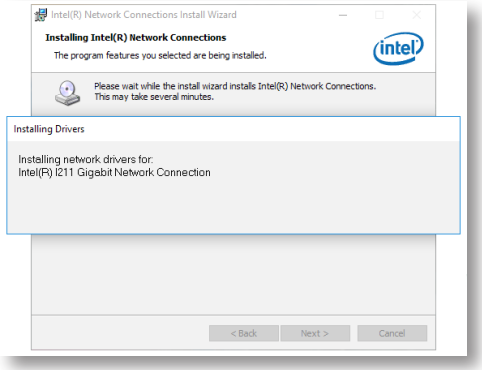
3. Select the program features you want installed then click “Next”.



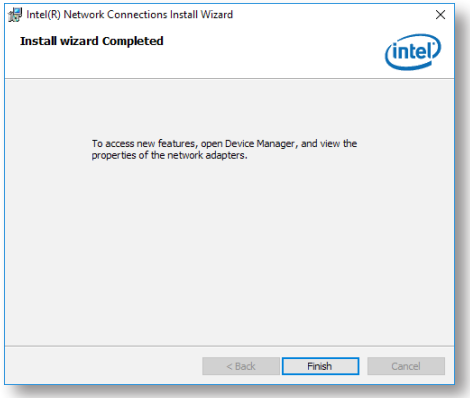
4. Click “Install” to begin the installation.



5. The step displays the installing status in the progress.

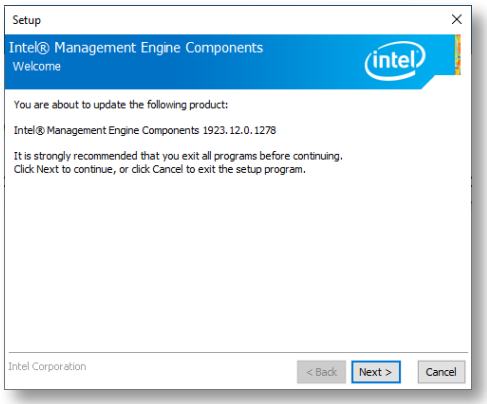


6. After completing installation, click “Finish”.

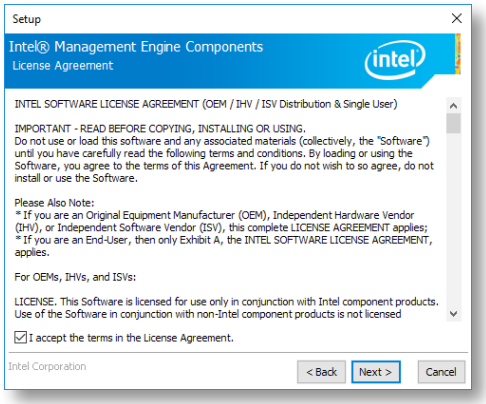


▶ Intel ME Drivers

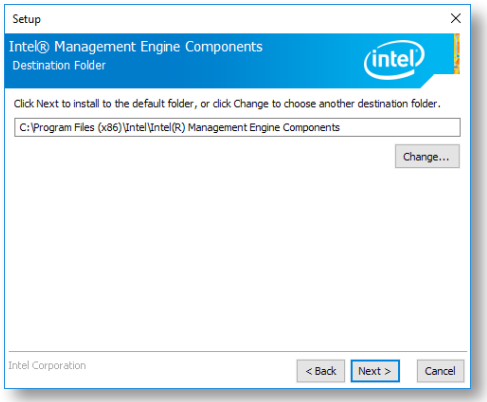
1. Setup is ready to install the driver. Click “Next”.



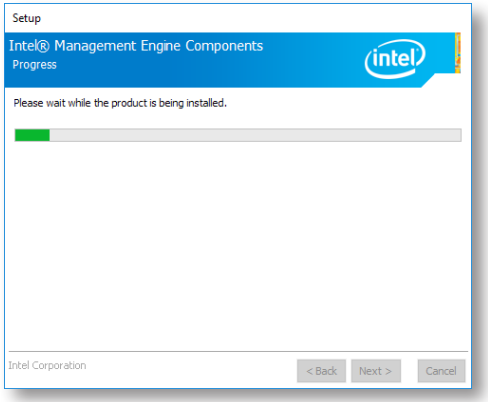
2. Read the license agreement then tick “I accept the terms in the License Agreement”. Click “Next”.



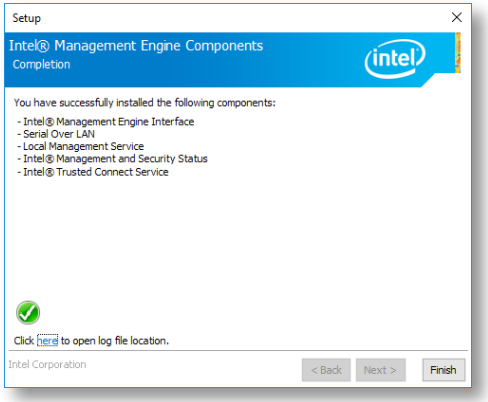
3. Click “Next” to install to the default folder, or click “Change” to choose another destination folder.



4. Please wait while the product is being installed.



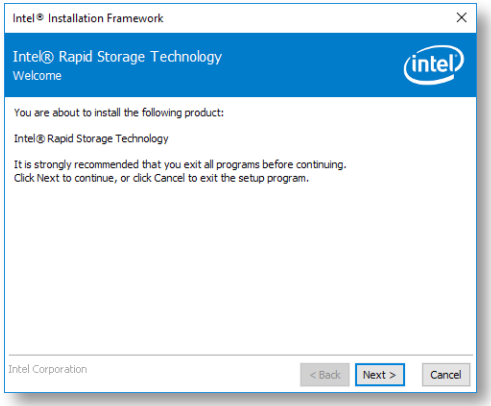
5. After completing installation, click “Finish”.



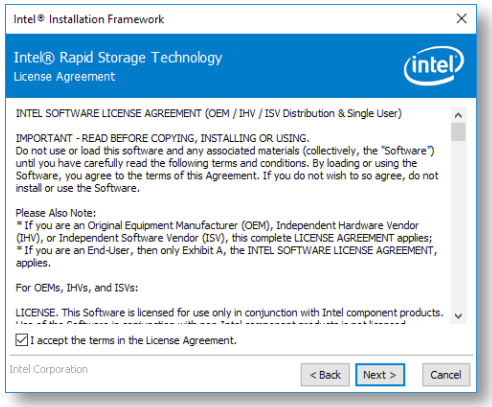
▶ Intel Rapid Storage Technology

The Intel Rapid Storage Technology is a utility that allows you to monitor the current status of the SATA drives. It enables enhanced performance and power management for the storage subsystem.

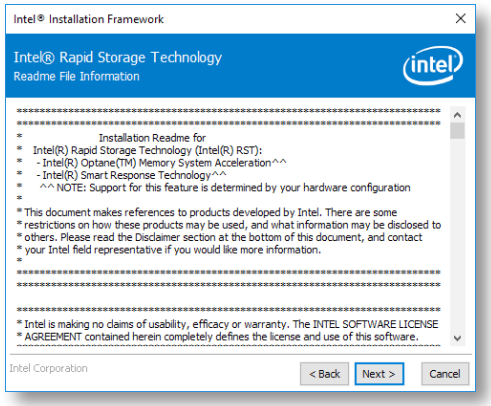
1. Setup is ready to install the utility. Click “Next”.



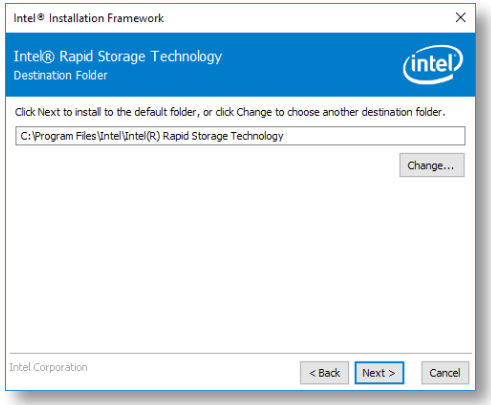
2. Read the license agreement and click “I accept the terms in the License Agreement”. Then, click “Next”.



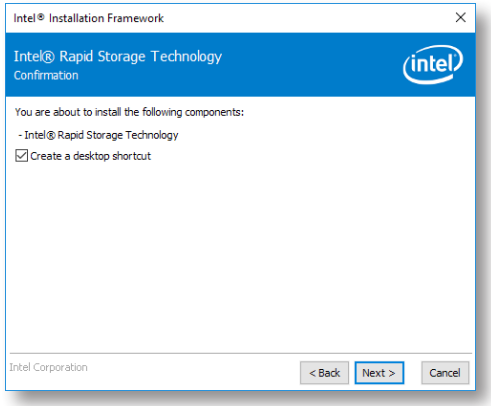
3. Go through the readme document to view system requirements and installation information then click “Next”.



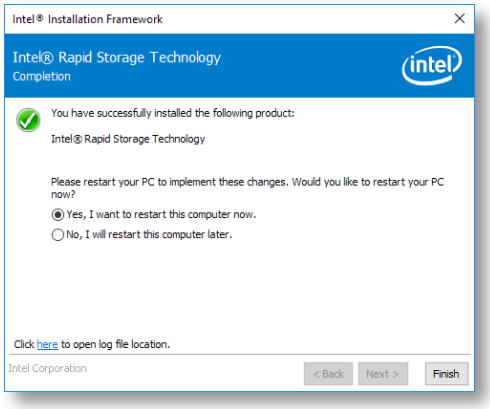
4. Click “Next” to install to the default folder or click “Change to choose another destination folder”.



5. Confirm the installation and click “Next”.

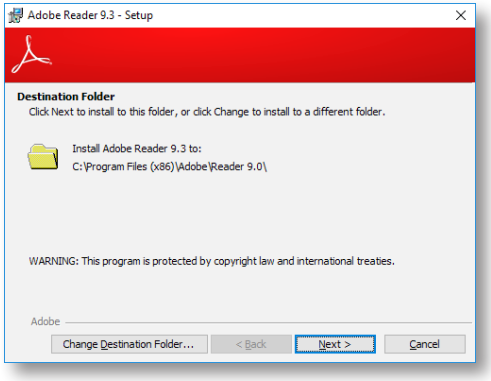


6. Click “Yes, I want to restart this computer now” to complete the installation and then click “Finish”.

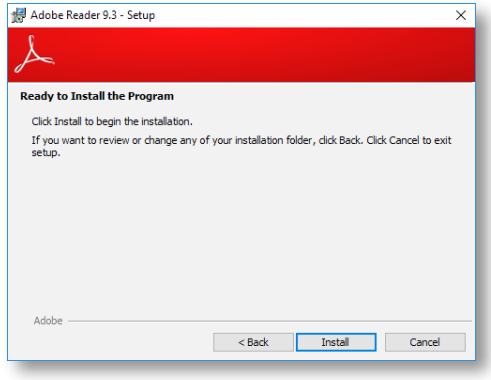


▶ Adobe Acrobat Reader 9.3

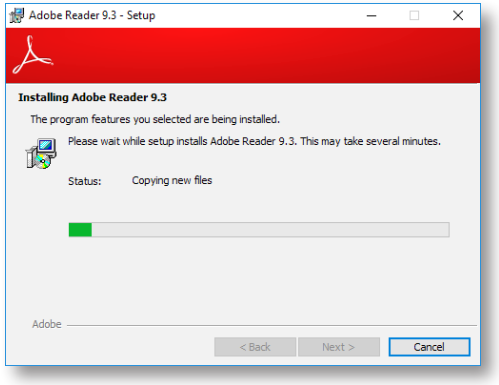
1. Click “Next” to install or click “Change Destination Folder” to select another folder.



2. Click “Install” to begin installation.



3. Setup is now installing the driver.



4. Click “Finish” to exit installation.